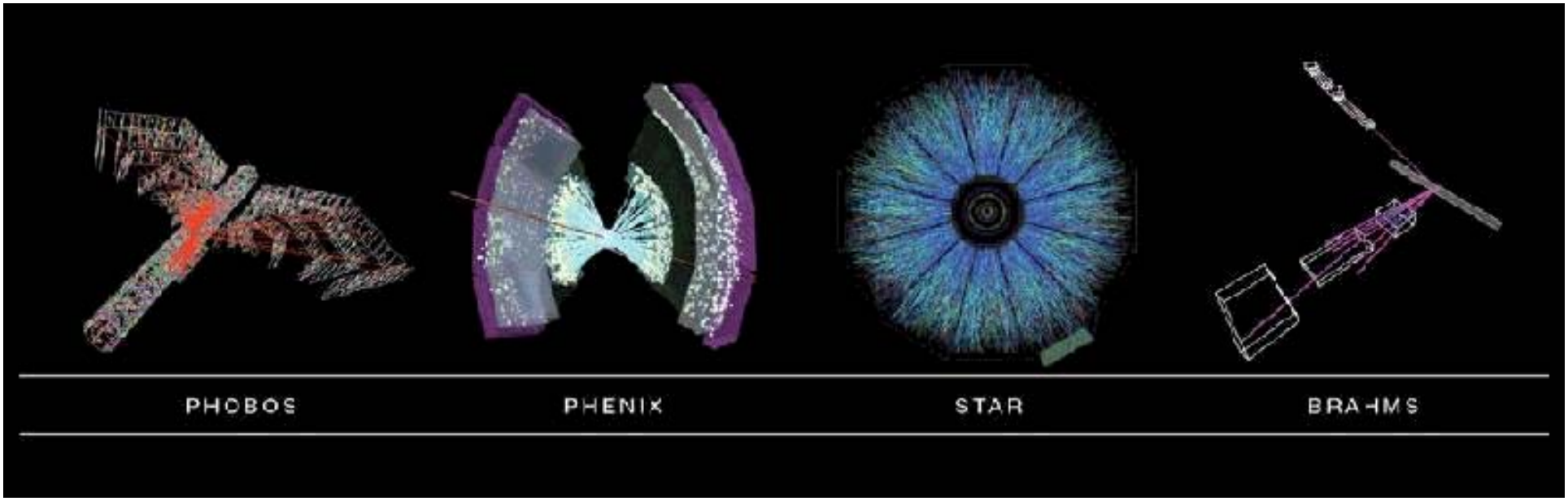
Semiconductor Vertex Tracking Convenor's Report

- What detector concepts are we trying to achieve and why
- Comparison of available technologies (focus on strip and drift)
- Past, present, future experiences
- What is possible ?
- What is realistic ?



- a small very high resolution vertexing device (STAR, PHOBOS)
- a mid-sized ‘spectrometer-matched’ vertex tracker (PHENIX)
- a very large tracking device (STAR)
- forward tracking disks or endcaps (STAR, PHENIX)

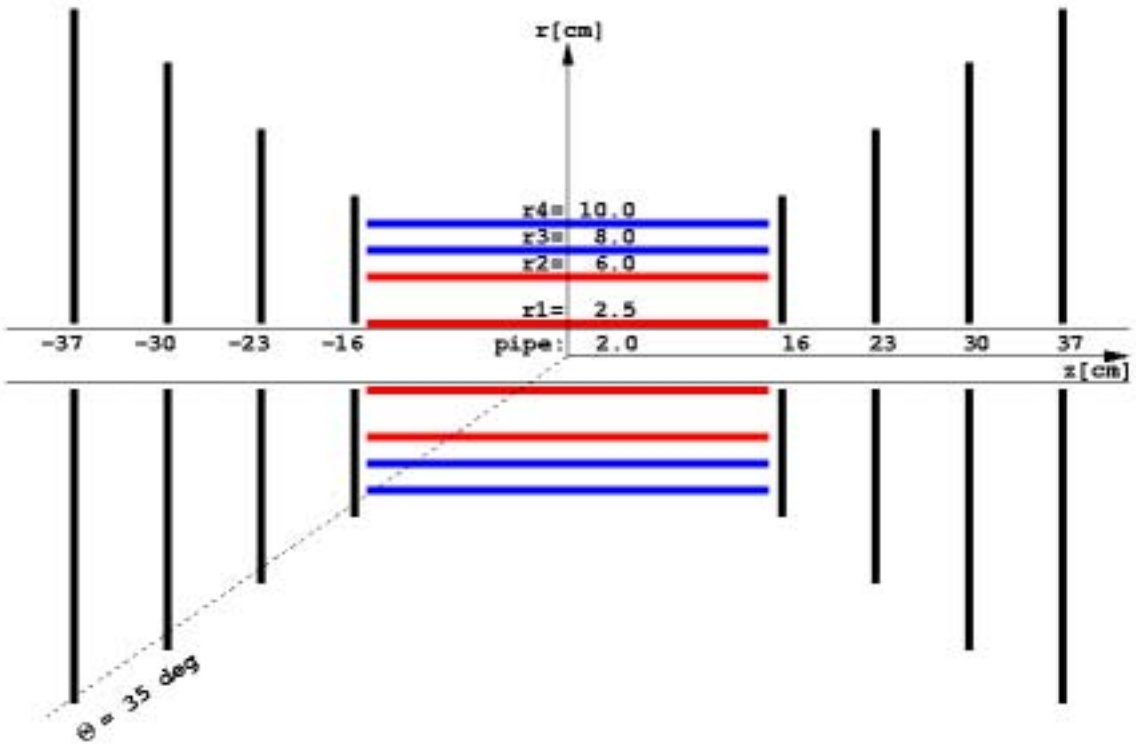
R. Bellwied, RHIC Workshop

Physics Goals

- D- and B-meson reconstruction in semi-leptonic and hadronic decay channels
- Tracking, particle identification and strange particle reconstruction covering up to 3 more rapidity units in forward direction
- Tracking equivalent or better than a TPC at central rapidities for higher luminosities and higher readout speed
- Potential triggering device at all trigger levels

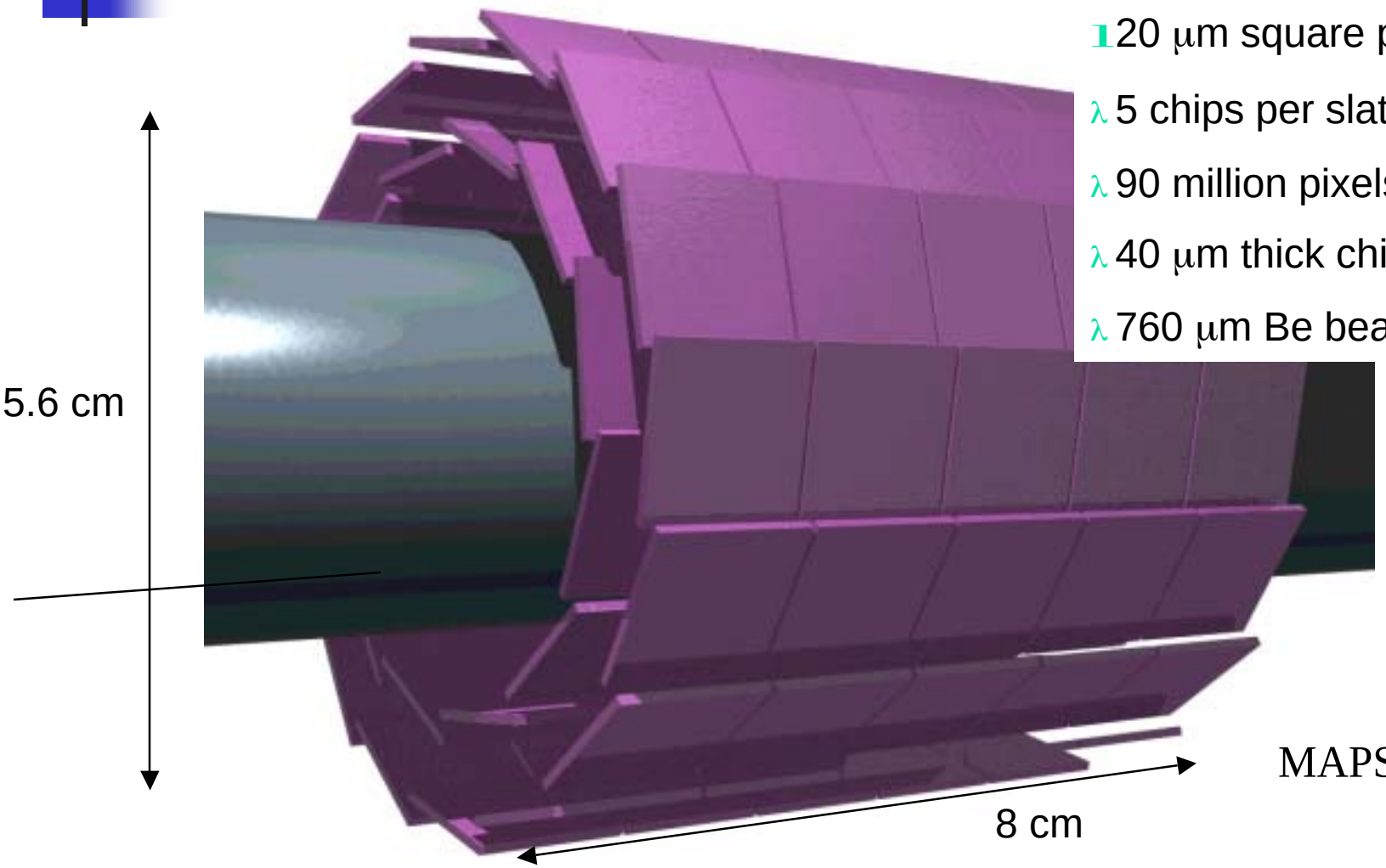
PHENIX Upgrade (for open charm+bottom)

- barrel plus endcap disks, technologies: strip and pixel
- 0.5 m^2 Si in barrel, ~1 m^2 Si in endcaps



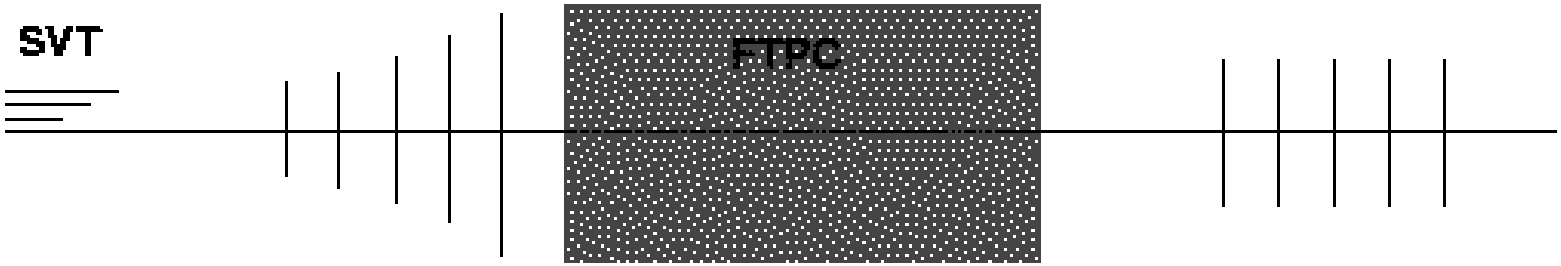
STAR Upgrade (for open charm)

- 20 μm square pixels
- 5 chips per slat
- 90 million pixels
- 40 μm thick chips
- 760 μm Be beam pipe



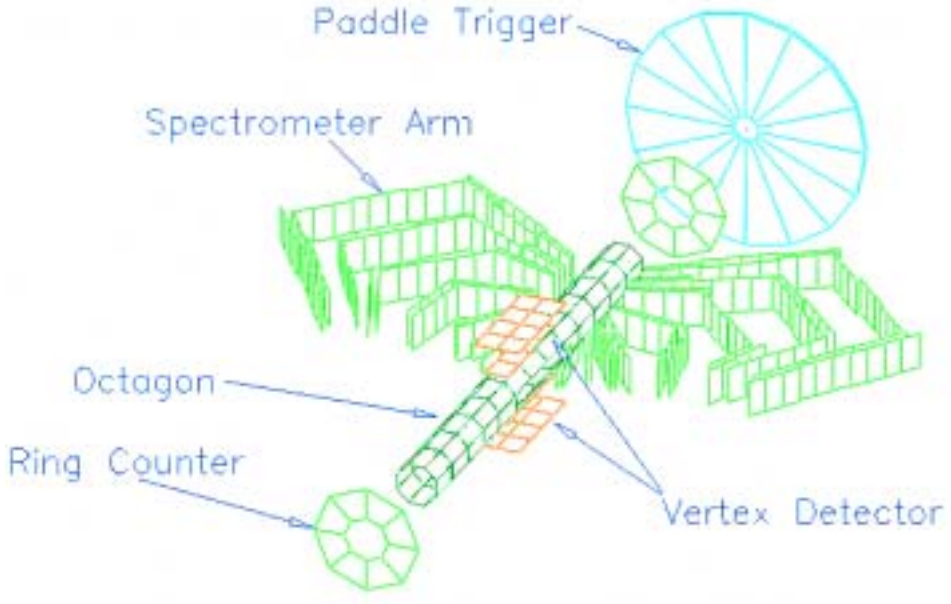
STAR Upgrade (for forward tracker)

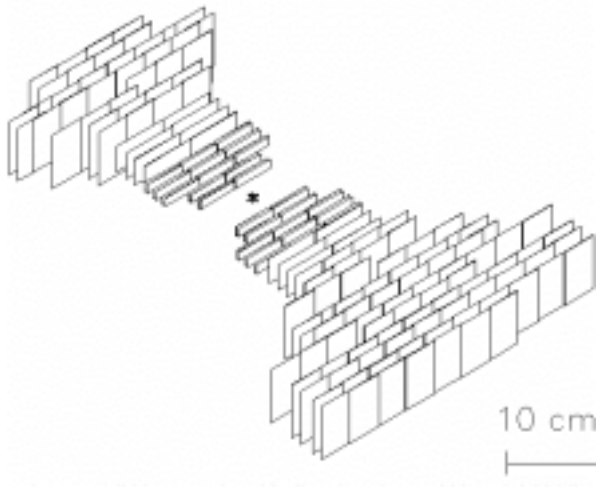
- Silicon forward disks, technology either: strip or hybrid pixel
- e.g. double-sided Silicon Strip detector, 100 micron pitch
- 5 by 5 cm active area, 1000 channels/wafer
- potential location:in front of FTPC
  - 5 layers (z=60,80,100,120,140 cm ; r=10,15,20,25,30 cm)
  - η = 2.3-4.0 (320,000 channels) (320 wafers, 0.8 m^2 of active Si)
- potential location: behind FTPC
  - 5 layers (z=350,375,400,425,450 cm ; r=20 cm all planes)
  - η = 3.5-5.0 (300,000 channels) (300 wafers, 0.75 m^2 of active Si)



PHOBOS Upgrade (for open charm)

- μvertex detector based on pads (10 layers) or pixels (5 layers)
- (106,496 channels if pad sensors)





STAR Upgrade (for central tracker)

- Silicon device to replace TPC, Technologies: drift or strip

Five layers of silicon drift detector
Radiation length / layer = 0.5 %
sigma_rphi = 7 μm, sigma_rz = 10 μm
44 m^2 Silicon
Wafer size: 10 by 10 cm
# of Wafers: 4500 (incl. spares)
# of Channels: 3,388,000 channels , (260 μm pitch)

Five layers of silicon strip detector
Radiation length / layer = 0.5 %
sigma_rphi = 10 μm, sigma_rz = ? μm
88 m^2 Silicon
Wafer size: 10 by 10 cm
# of Wafers: 9000 (incl. spares)
# of Channels: 27,104,000 channels , (65 μm

Layer Radii	Half-lengths
25.00 cm	25.00 cm
50.00 cm	50.00 cm
75.00 cm	75.00 cm
100.00 cm	100.00 cm
125.00 cm	125.00 cm

(projected cost: $25-30 Million)

R. Bellwied, RHIC Workshop

Available Technologies

- Charged Coupled Devices (CCD)
- Monolithic Active Pixel Sensors (MAPS)
- Hybrid Pixel Sensors
- Silicon Drift Detectors (SDD)
- Silicon Strip Detectors
- Others: Diamond, GaAs, Silicon Pad, etc.

What has been constructed

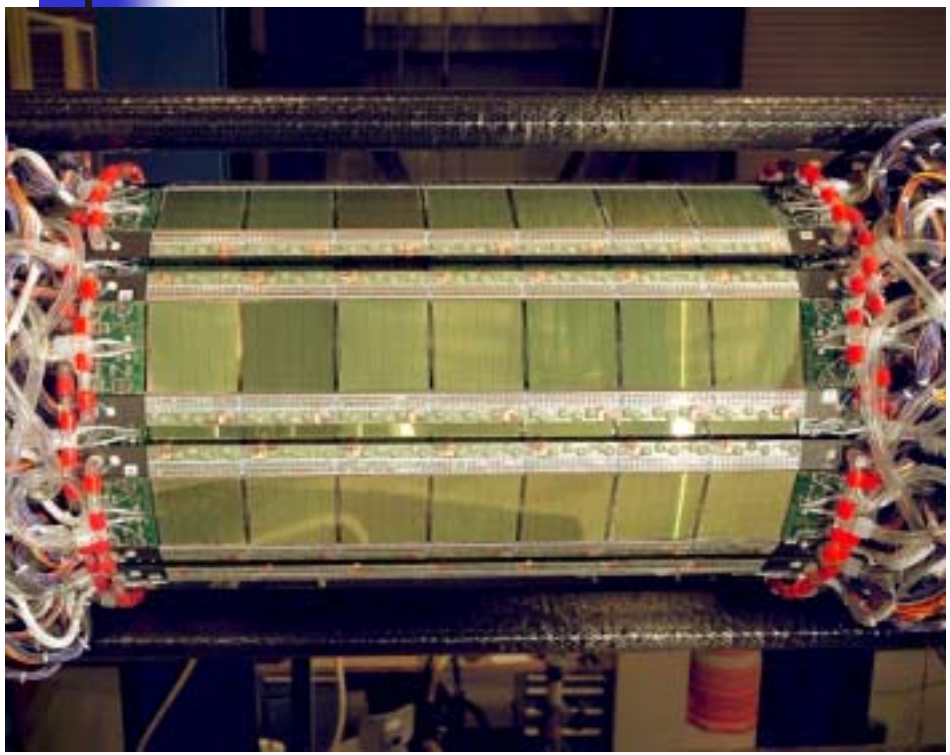
- CCD: SLAC-SLD
- SDD: RHIC-STAR
- Strip: CLEO, H1, HERA-B, ZEUS, D0 BABAR, CDF, ALEPH, DELPHI, BELLE, etc.
- Hybrid Pixel: - (SPS-WA97)
- MAPS: -

CCD - VXD3 at SLAC

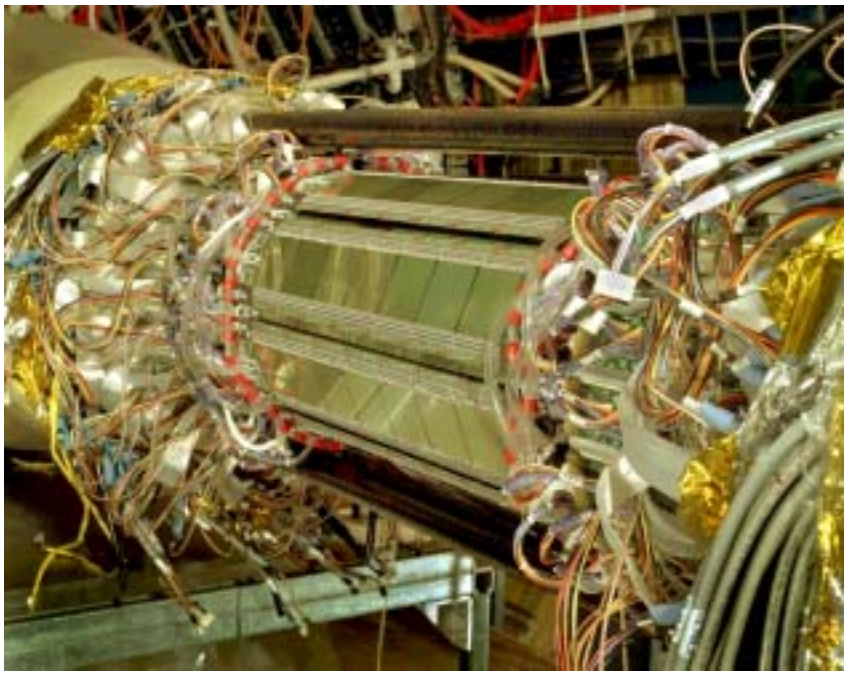
- Very thin, 0.4% radiation length
- High resolution
  - pixels - 20 μm cubes
  - surface resolution < 4 μm
  - projected impact parameter resolution 11 μm
- Close to beam, inner layer at 2.8 cm radius
- 307 million pixels, < 1 cent/pixel

R. Bellwied, Snowmass 2001

The SVT in STAR

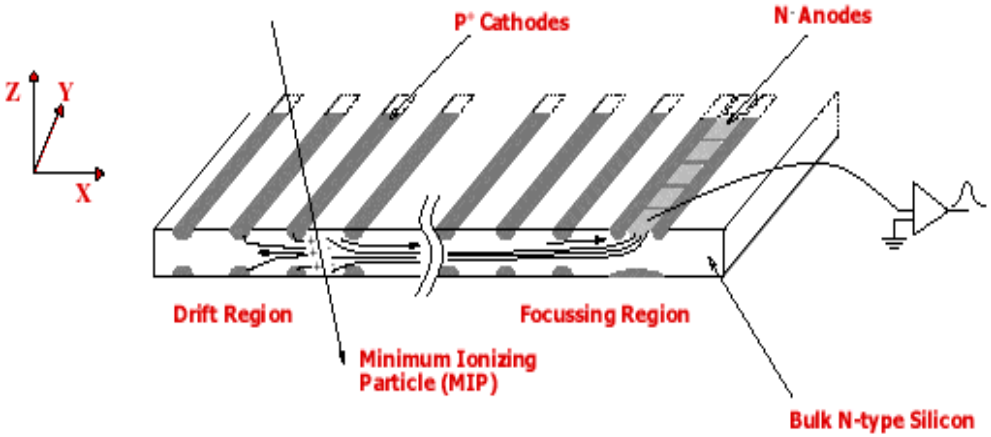


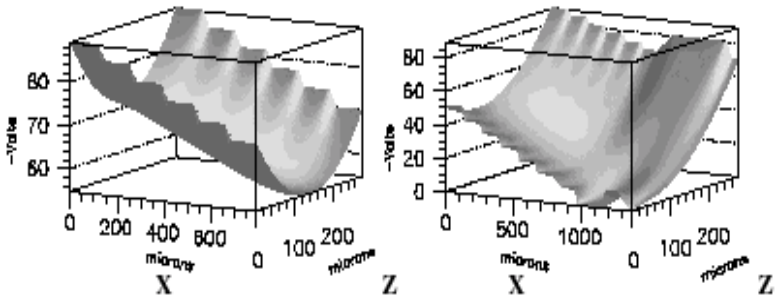
The final device….



… and all its connections

SDD's: 3-d measuring devices





--Drift time determines 'X' coordinate
--Hit anodes determine 'Y' coordinate

E. Gatti, P. Rehak, and J. Walton, NIM 226 (1984) 129.

Features

- Position resolutions in both anode and drift directions < 20 microns
- Low capacitance anodes (low noise)
- High density tracking (pixel-like readout)
- Low number of readout channels
- Switched Capacitor Array readout for drift time
- Silicon is 4in Wacker NTD material

Present status of technology

STAR

- 4in. NTD material, 3 kΩcm, 280 μm thick, 6.3 by 6.3 cm area
- 250 μm readout pitch, 61,440 pixels per detector
- SINTEF produced 250 good wafers (70% yield)

ALICE

- 6in. NTD material, 2 kΩcm, 280 μm thick, 280 μm pitch
- CANBERRA produced around 100 prototypes, good yield

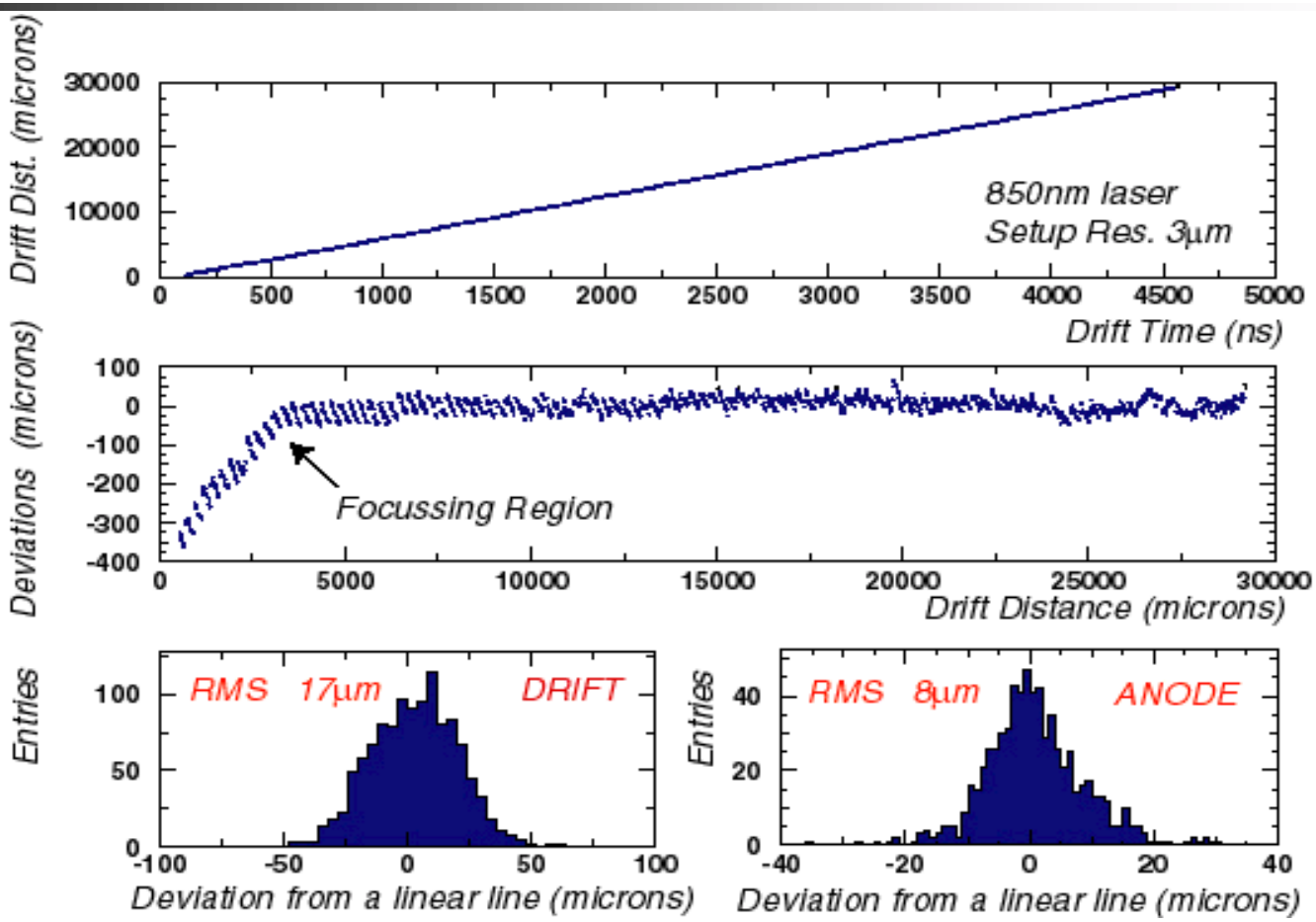
Future

- 6in. NTD, 150 micron thick, any pitch between 200-400 μm
- 10 by 10 cm wafer

STAR-SVT characteristics

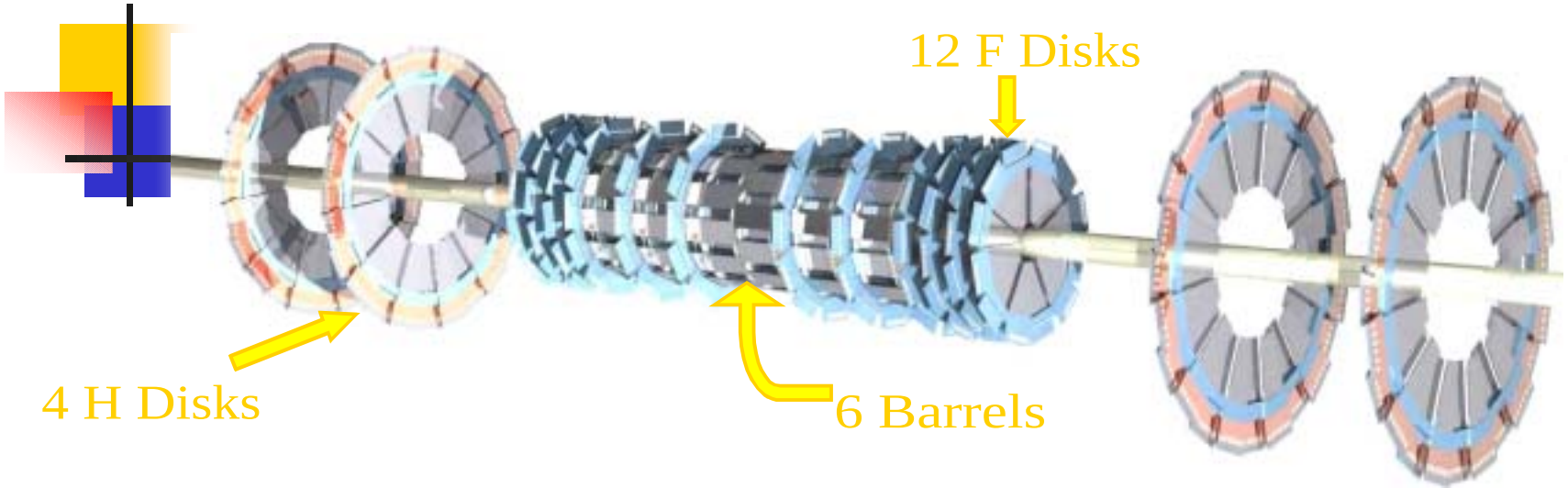
- 216 wafers (bi-directional drift) = 432 hybrids
- 3 barrels, r = 5, 10, 15 cm, 103,680 channels, 13,271,040 pixels
- 6 by 6 cm active area = max. 3 cm drift, 3 mm (inactive) guard area
- max. HV = 1500 V, max. drift time = 5 μs, (TPC drift time = 50 μs)
- anode pitch = 250 μm, cathode pitch = 150 μm
- SVT cost: $7M for 0.7m² of silicon
- Radiation length: 1.4% per layer
  - 0.3% silicon, 0.5% FEE (Front End Electronics),
  - 0.6% cooling and support. Beryllium support structure.
  - FEE placed beside wafers. Water cooling.

Typical SDD Resolution

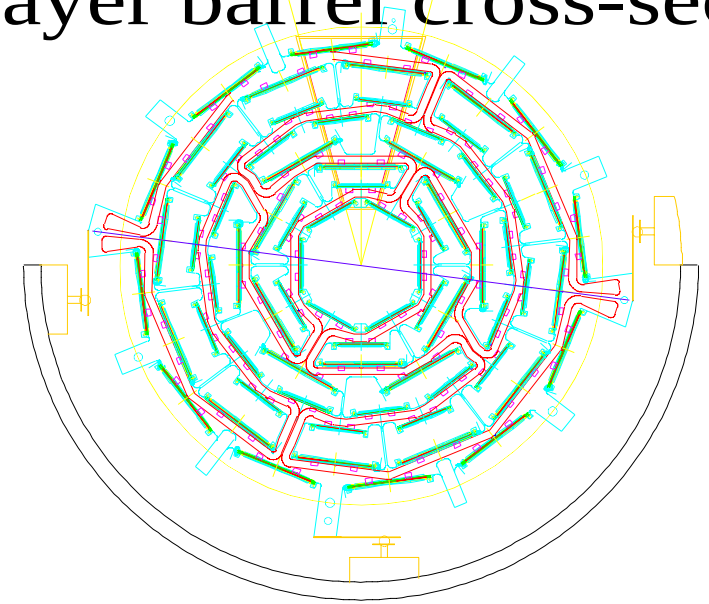


R. Bellwied, Snowmass 2001

SMT Design (CDF Upgrade)



4-layer barrel cross-section



SMT Statistics

	Barrels	F-Disks	H-Disks
Channels	387072	258048	147456
Modules	432	144	96
Si Area	1.3 m^2	0.4 m^2	1.3 m^2
Inner R	2.7 cm	2.6 cm	9.5 cm
Outer R	9.4 cm	10.5 cm	26 cm

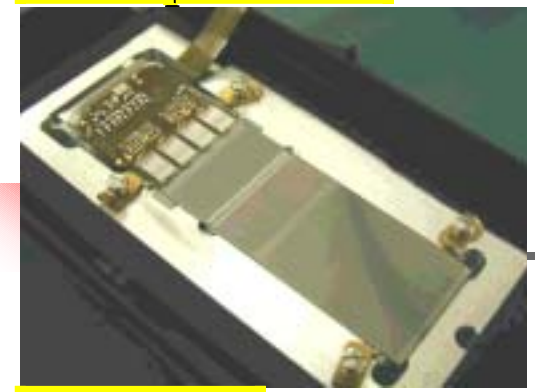
Detector Specifications (2)

CDF	Layer 00	SVX II	ISL	Totals
Layers	1	5	2	8
Length	0.9 m	0.9 m	1.9 m	
Channels	**13824**	**405504**	**303104**	**722432**
Modules	48 SS	360 DS	296 DS	704
Readout Length	14.8 cm	14.5 cm	21.5 cm	
Inner Radius	1.35 cm	2.5 cm	20 cm	1.35 cm
Outer Radius	1.65 cm	10.6 cm	28 cm	28 cm
Power	~100 W	1.4 kW	1.0 kW	2.5 kW

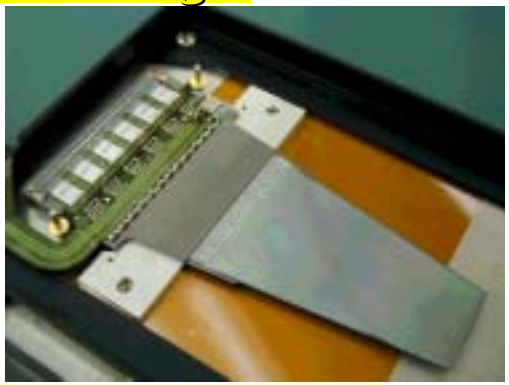
6m2 of silicon, 376 modules, 722432 RO channels

CDF Production & Assembly: Devices

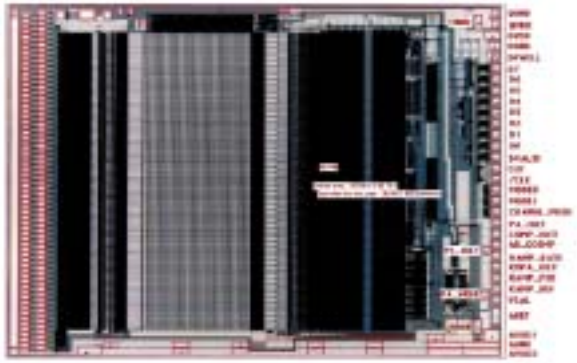
9-chip ladder



H wedge



SVX IIe chip

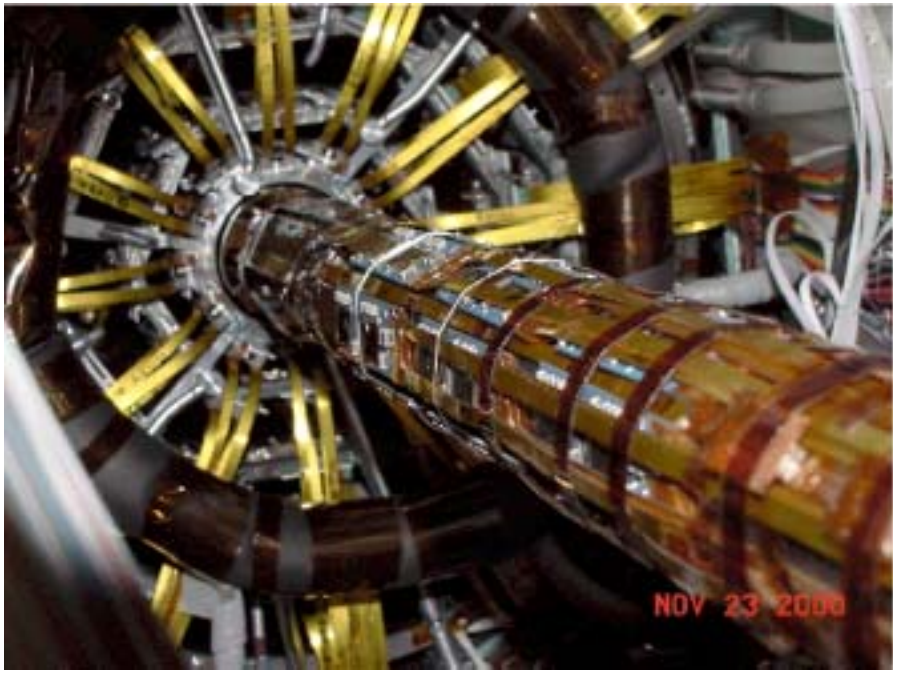


- Ladders
  - 3-chip: 72 single-sided, axial ladders in the two outer barrels
  - 6-chip: 144 double-sided, axial/90° ladders in the four inner barrels
  - 9-chip: 216 double-sided, axial/2° ladders in all barrels
  - Ladders have a mechanical accuracy of 2-5 μm
- Wedges
  - F Disks: 144 double-sided, ±15°, 6+8 chip wedges
  - H Disks: 96_2 back-to-back single-sided, ±7.5°, 6 chip wedges
  - Wedges have a mechanical accuracy of 5-10 μm

SVX IIe chip

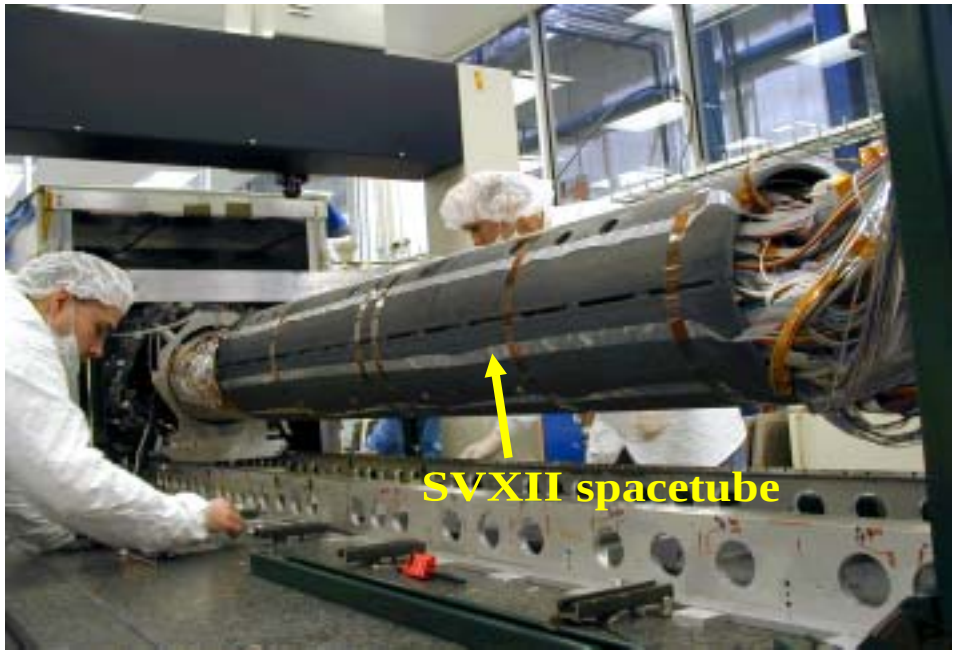
- 128 channel 8-bit digital chip, with 32 cell pipeline depth
- 1.2 μm rad-hard technology
- 106 MHz digitization, 53 MHz readout
- Rise time set to integrate 99% of charge in 100 ns
- Over 2.3 million wirebonds were made to chips

Final Assembly

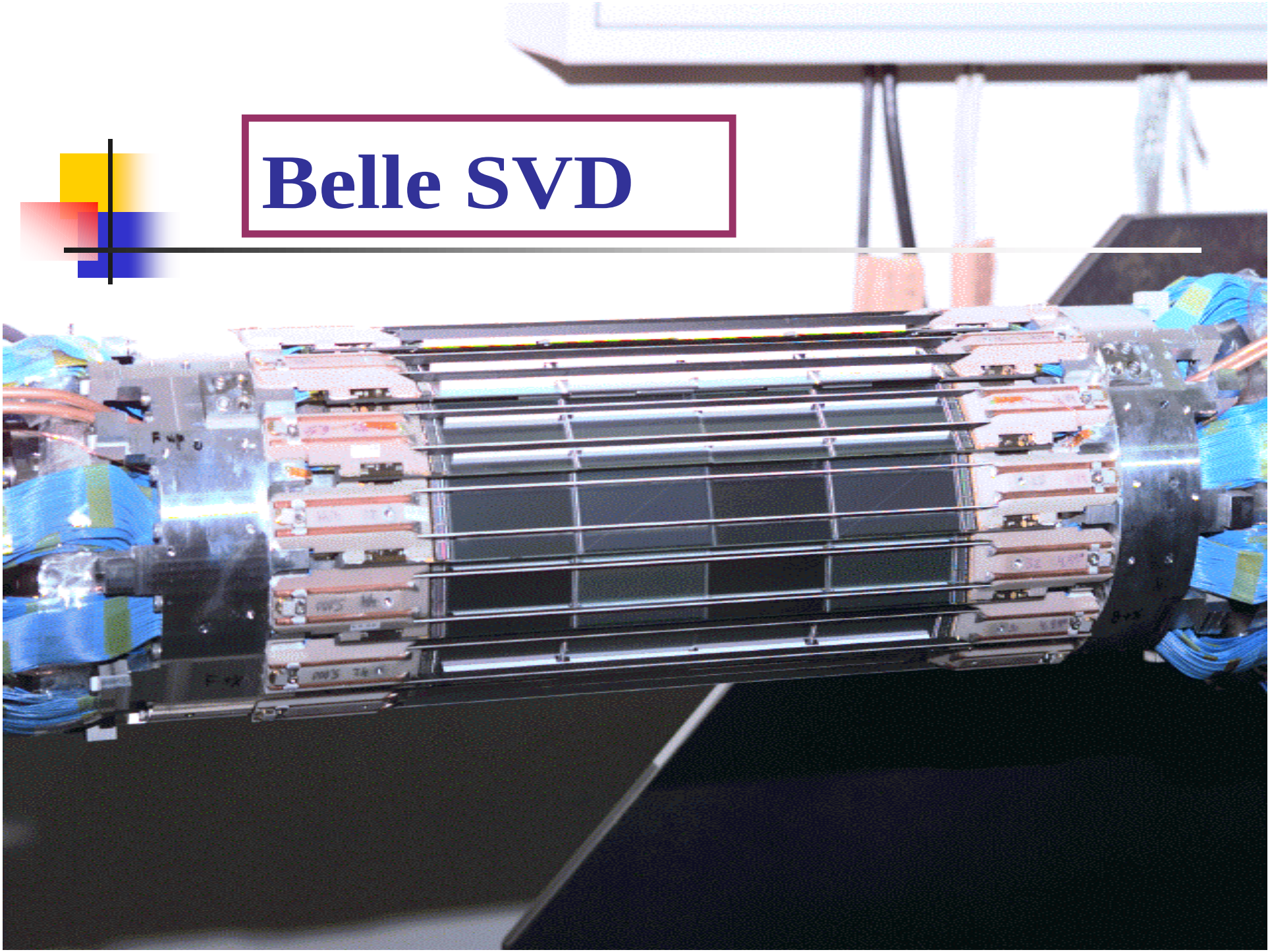


Only 300-450μm clearance for insertion of L00 into SVXII !

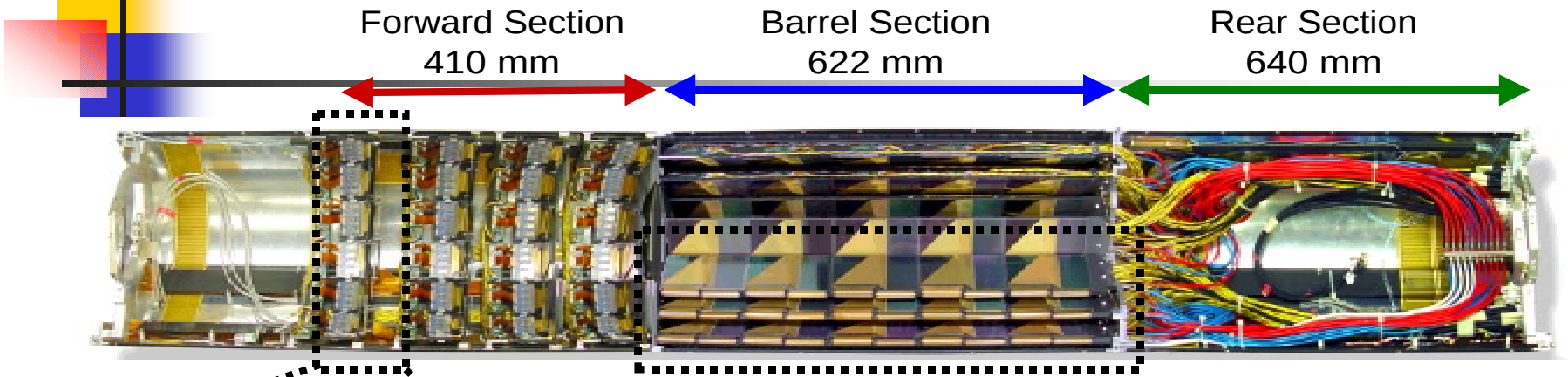
7-15mm clearance for insertion of SVXII into ISL

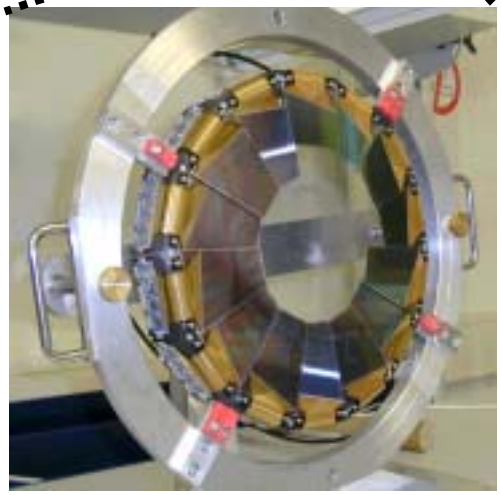


Belle SVD



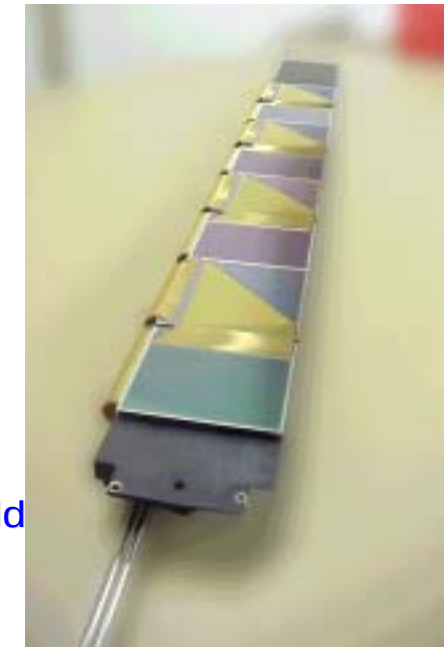
The ZEUS-MVD layout





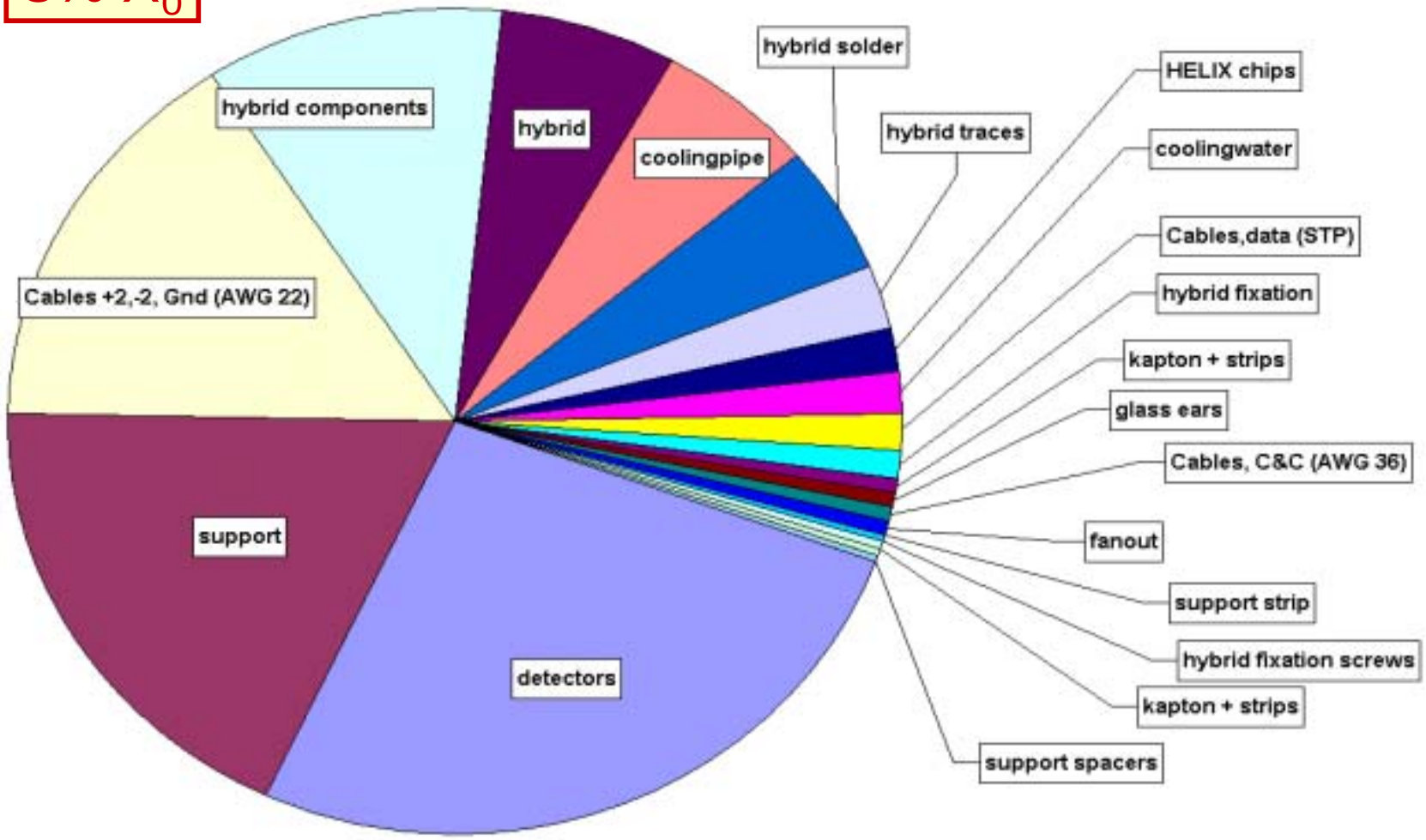
The forward section counts 4 wheels, each one composed by 2 layers of 14 trapezoidal detectors

The barrel section has 3 layers of ladders, support frames which hold 5 full modules

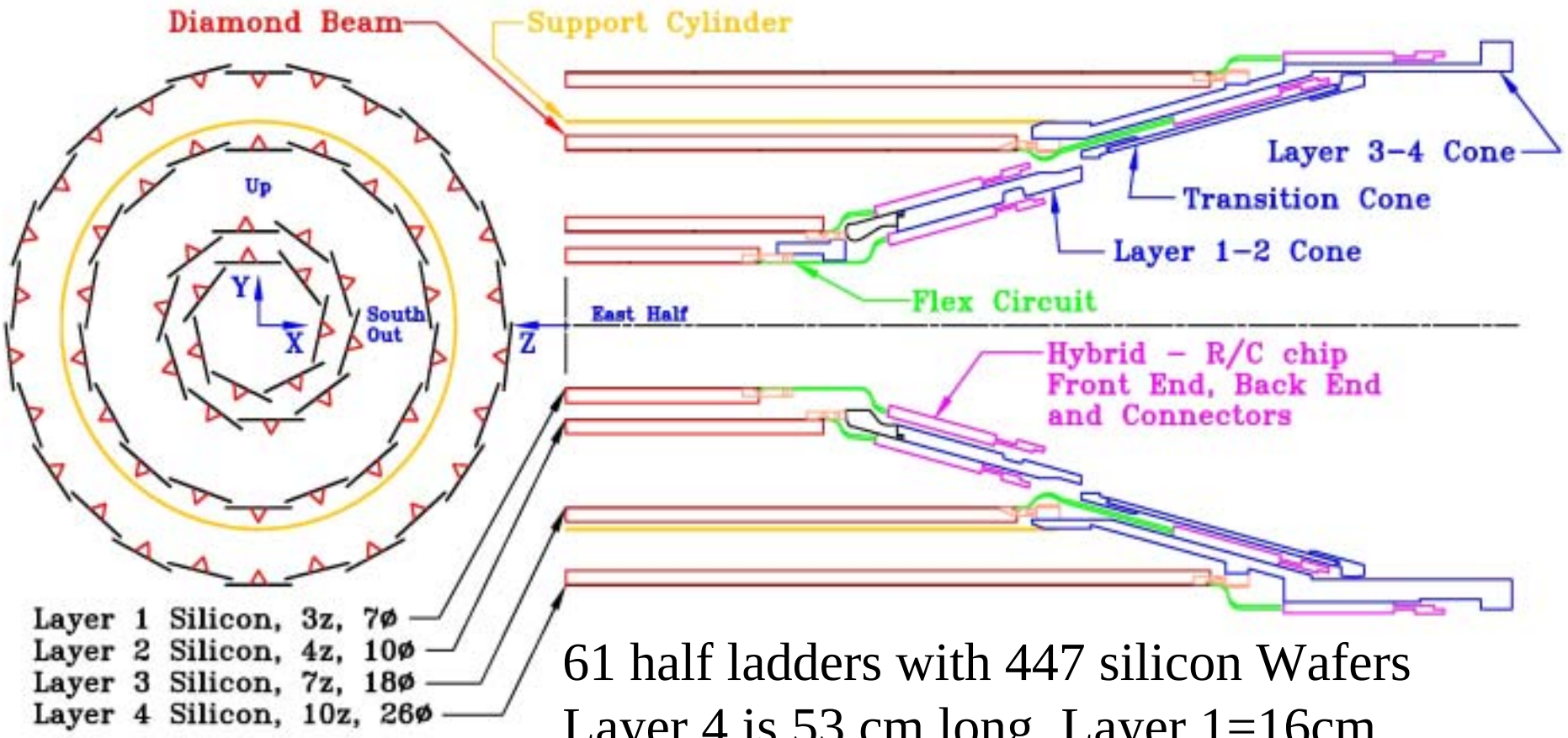


Material in a ladder

3% X_0



CLEO Mechanical Design



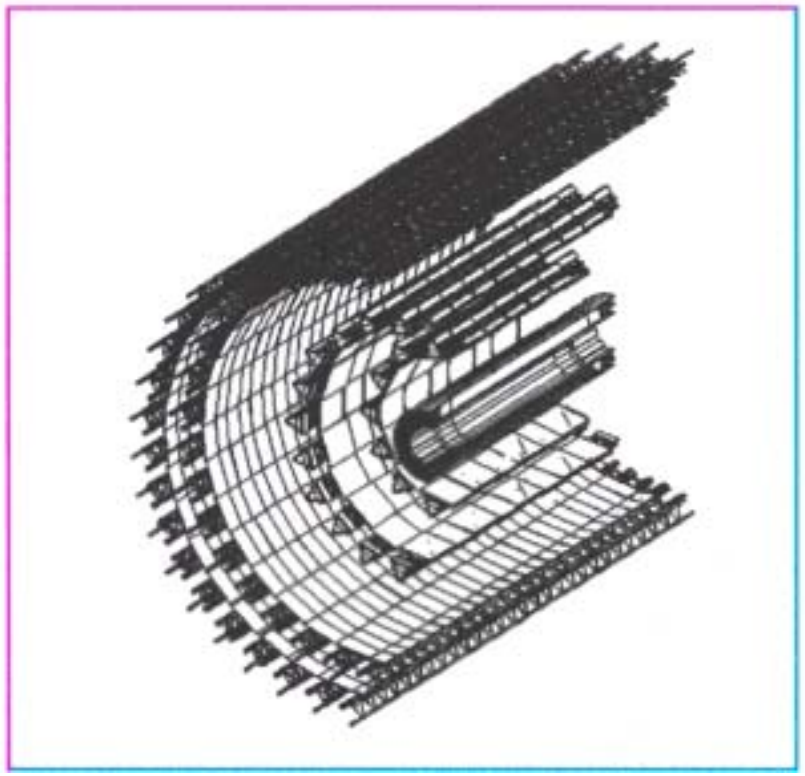
61 half ladders with 447 silicon Wafers

Layer 4 is 53 cm long, Layer 1=16cm

What is being constructed ?

- CCD: -
- SDD: ALICE
- Strip: ATLAS, CMS, ALICE
- Hybrid Pixel: ATLAS, CMS, ALICE
- MAPS: -

ALICE Inner Tracking System (ITS)

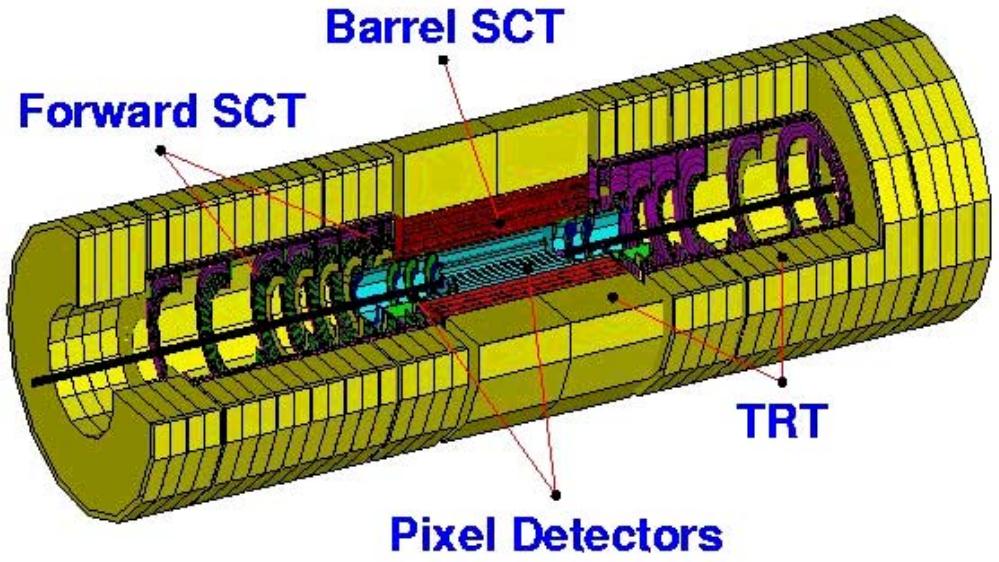


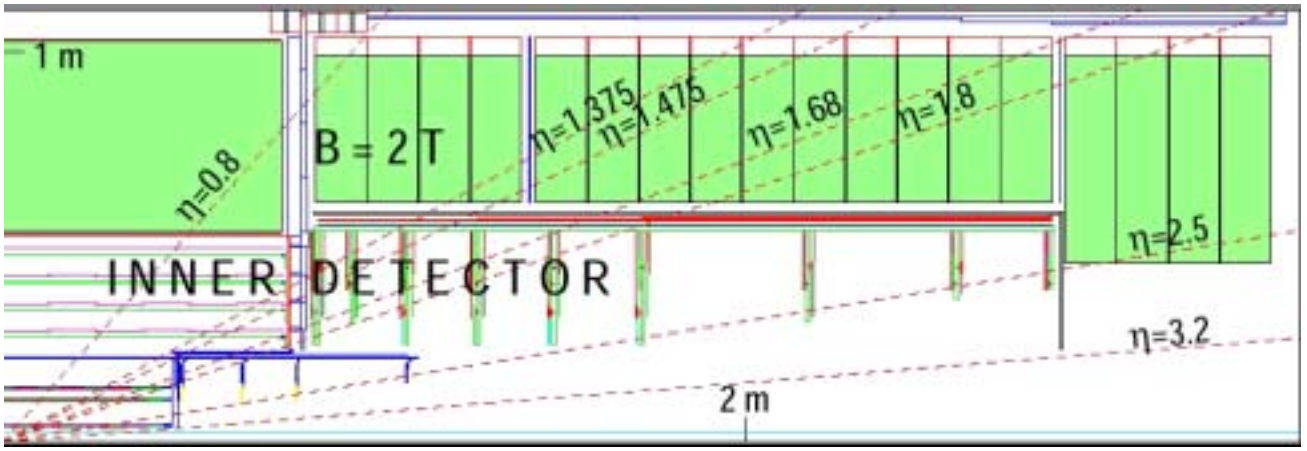
Layer	Type	r (mm)	area (m^2)	channels	rϕ res (μm)	z res (μm)
1	Pixel	**40**	**0.09**	5 242 880	**12**	
2	Pixel	**70**	**0.18**	10 485 760	**12**	
3	Drift	**149**	**0.37**	43 008	**38**	
4	Drift	**238**	**0.89**	90 112	**38**	
5	Strip	**391**	**2.28**	1 201 152	**20**	830
6	Strip	**436**	**2.88**	1 517 568	**20**	830

ATLAS - SCT in the Inner Detector

SCT:

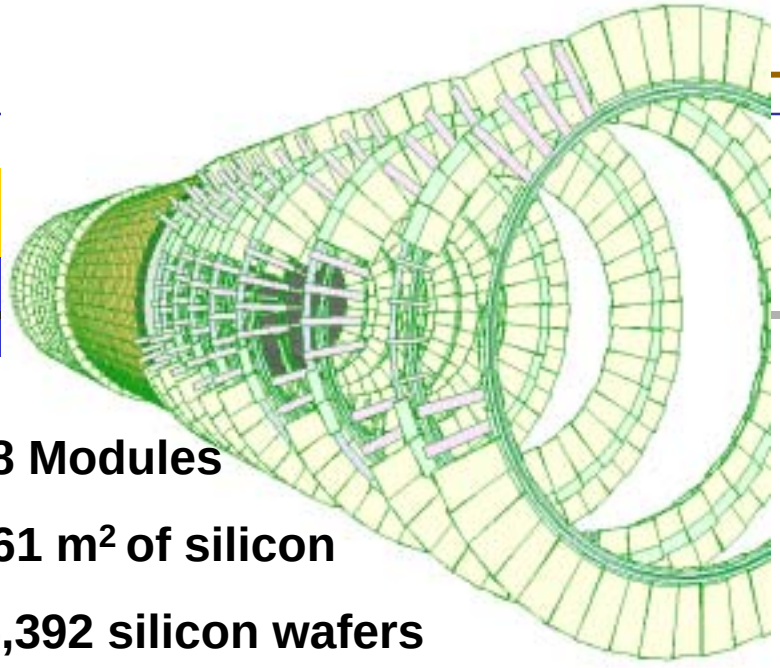
- **4 Barrels + 2x9 wheels**
- **4 different module types in the wheels**
- $\eta < 2.5$





ATLAS SCT

The SCT Semiconductor Tracker



Barrel diameters:

B3: 568 mm

B4: 710 mm

B5: 854 mm

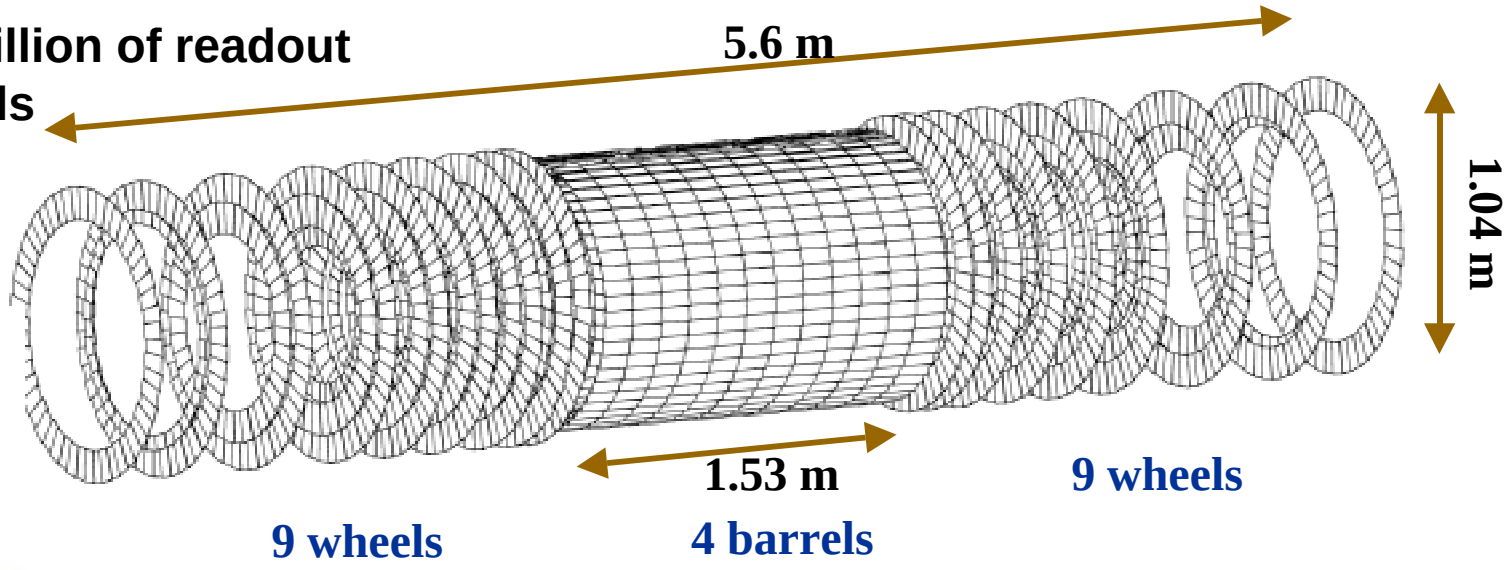
B6: 996 mm

4088 Modules

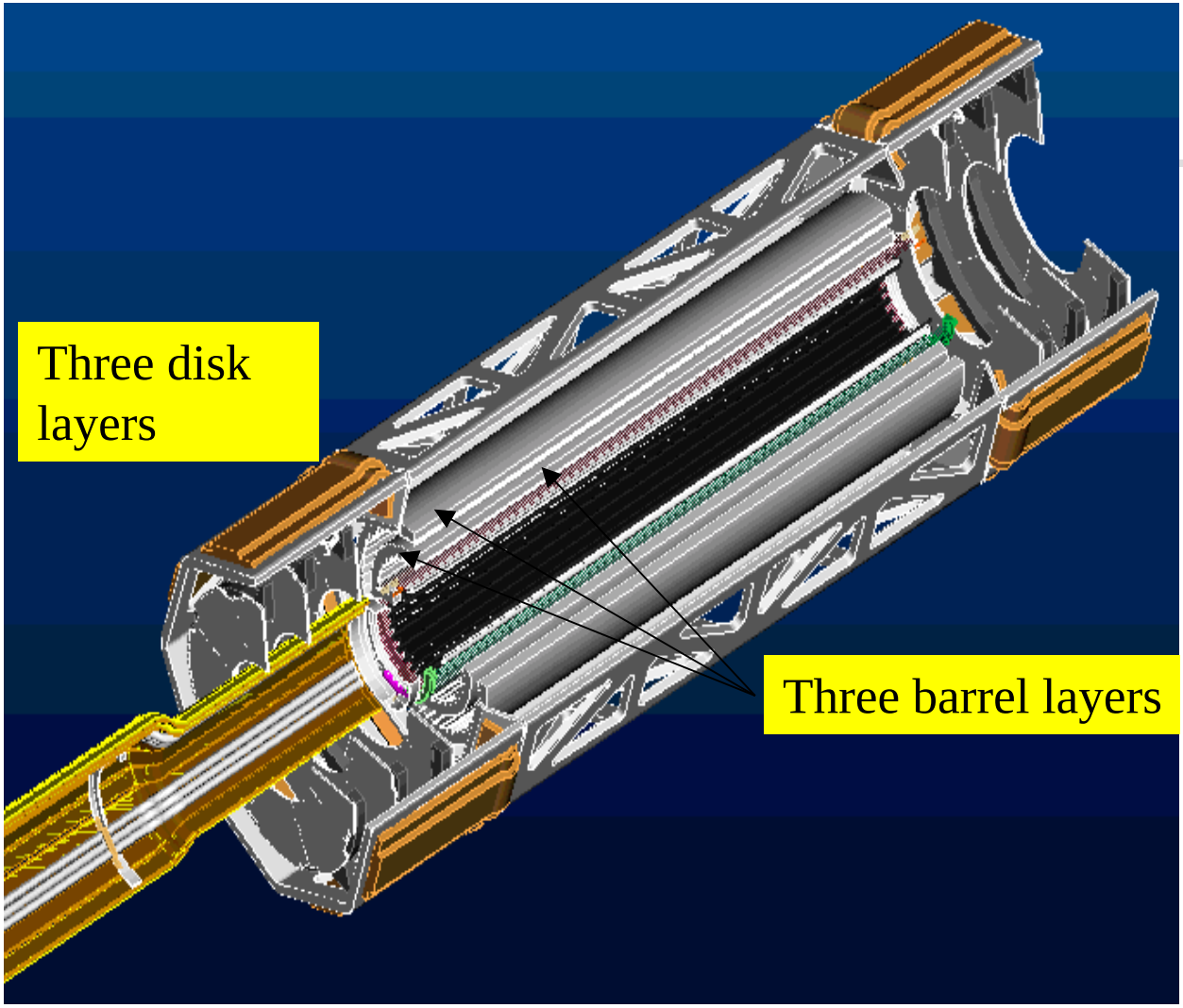
~ 61 m² of silicon

15,392 silicon wafers

~ 6.3 million of readout channels



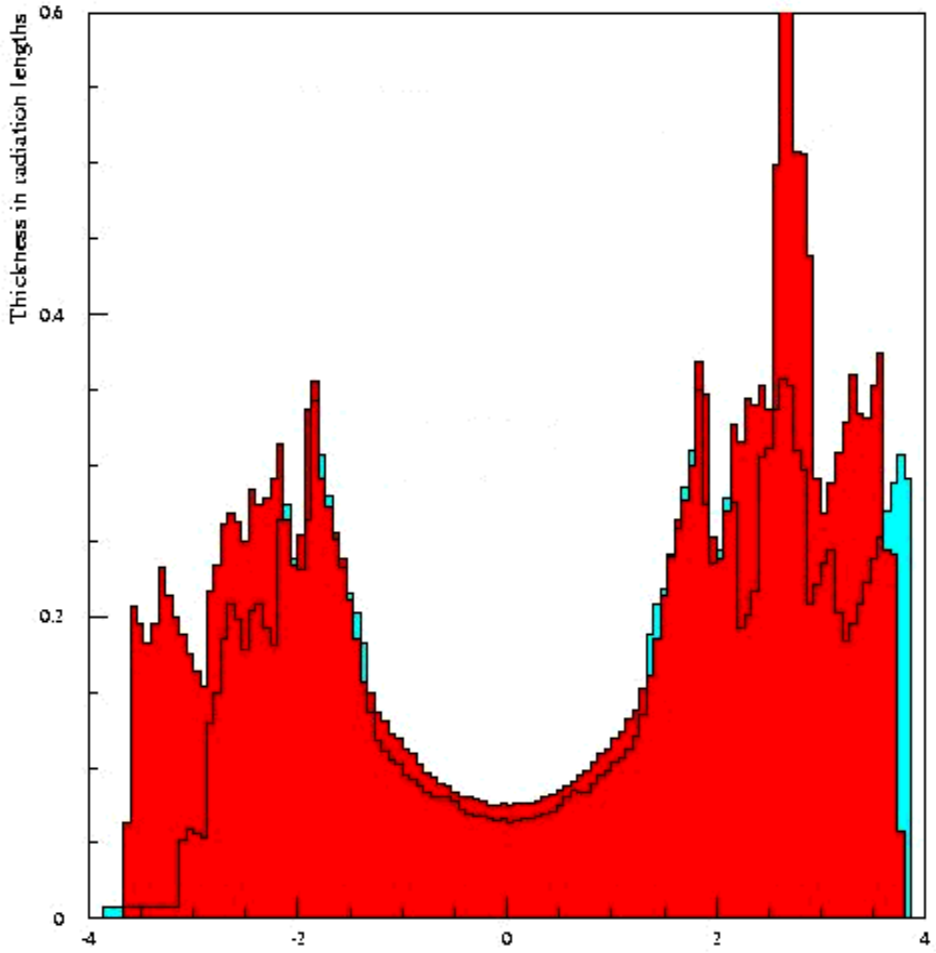
The ATLAS Pixel Detector



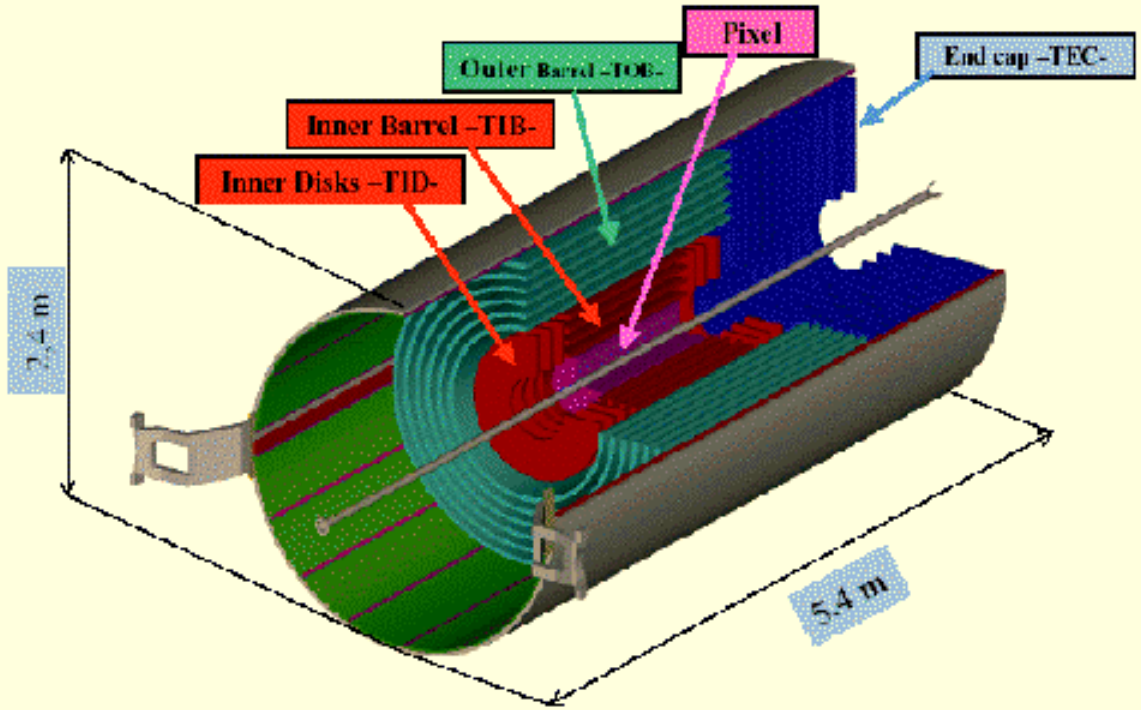
- It is the innermost part of the silicon vertex tracker of the ATLAS experiment.
- It consists of two parts:
  - 3 barrel layers
  - 3+3 forward-backward disks
- ~2.0 m^2 of sensitive area with 0.8×10^8 channels
- 50 μm × 400 μm silicon pixels (50 μm × 300 μm in the B-layer)

Material budget for ATLAS

- To minimize material:
  - 250 μm thick sensor;
  - Electronics thinned to 150 μm;
  - all supports in carbon composite material: it is ultra stable and ultra light (~4.4Kg)
- Asymmetric distribution of material: B-layer services exit on one side.



Layout



- 4 layers in TIB
- 6 disks in TID
- 6 layers in TOB
- 18 disks in TEC

24 m^3 kept at a temperature of –10 °C

Matteo M. Angarano
Università di Perugia

Numbers for the CMS tracker

6,136 thin sensors (320 μm), 18,192 thick sensors (500 μm)

6,136 thin detectors (1 sensor), 9,096 thick detectors (2 sensors)

3,122 + 1,512 thin modules (ss + ds)

5,496 + 1,800 thick modules (ss + ds)

9,648,128 strips = electronics channel

75,376 APV chips subμ = 25,000,000 bonds

440 m^2 of silicon wafers, 210 m^2 of silicon sensors

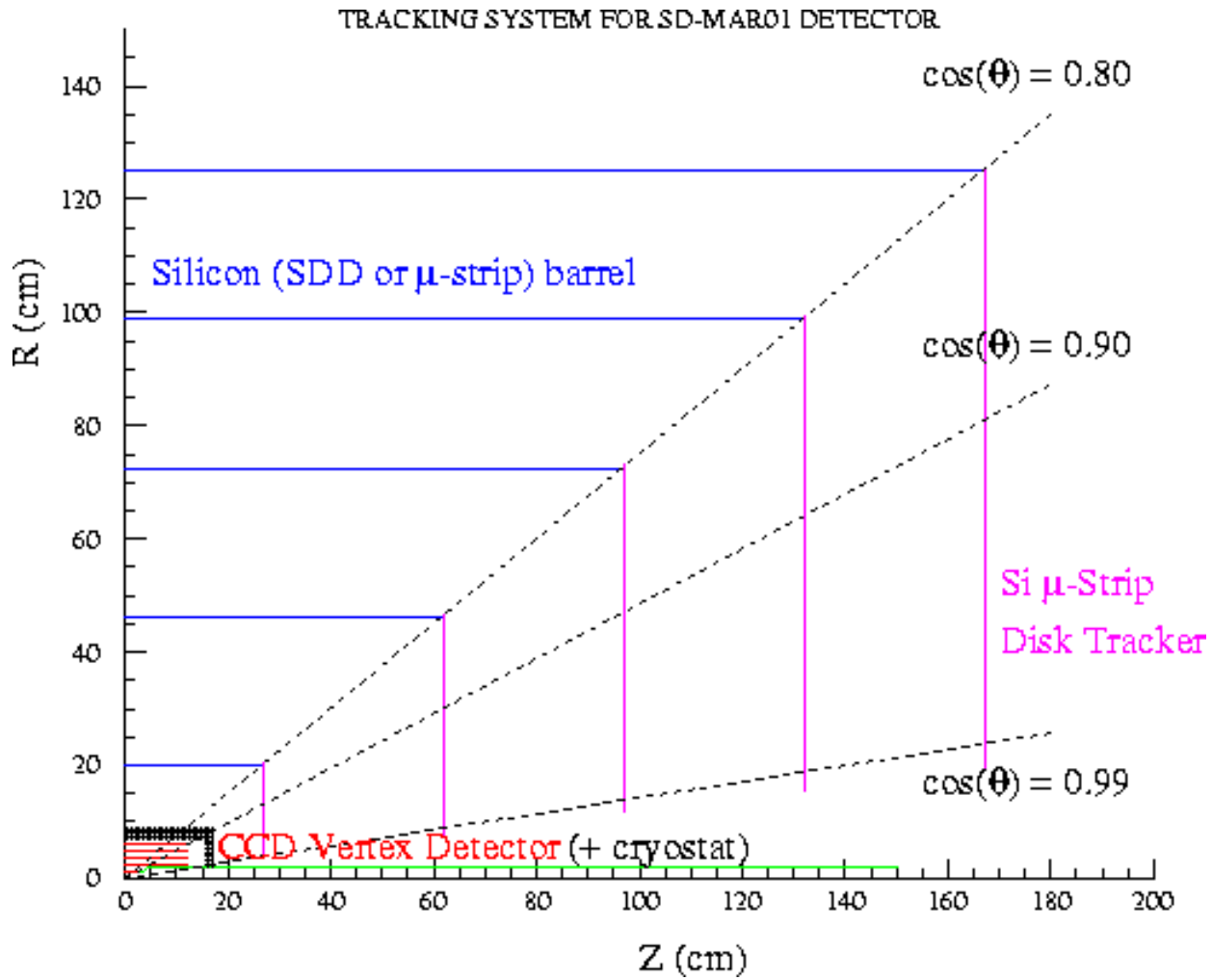
14 sensor geometries

Strip length ranges from 9 to 21 cm

What is being proposed?

- CCD: LC, RHIC
- SDD: LC, RHIC
- Strip: BTeV, LHCb, LC, RHIC
- Hybrid Pixel: BTeV, RHIC
- MAPS: RHIC

Silicon detector option for LCD



Silicon detector option for LCD (small detector, high field B=5T)

Central tracker: Silicon Drift Detectors
Five layers
Radiation length / layer = 0.5 %
sigma_rphi = 7 μm, sigma_rz = 10 μm

Layer Radii	Half-lengths
20.00 cm	26.67 cm
46.25 cm	61.67 cm
72.50 cm	96.67 cm
98.75 cm	131.67 cm
125.00 cm	166.67 cm

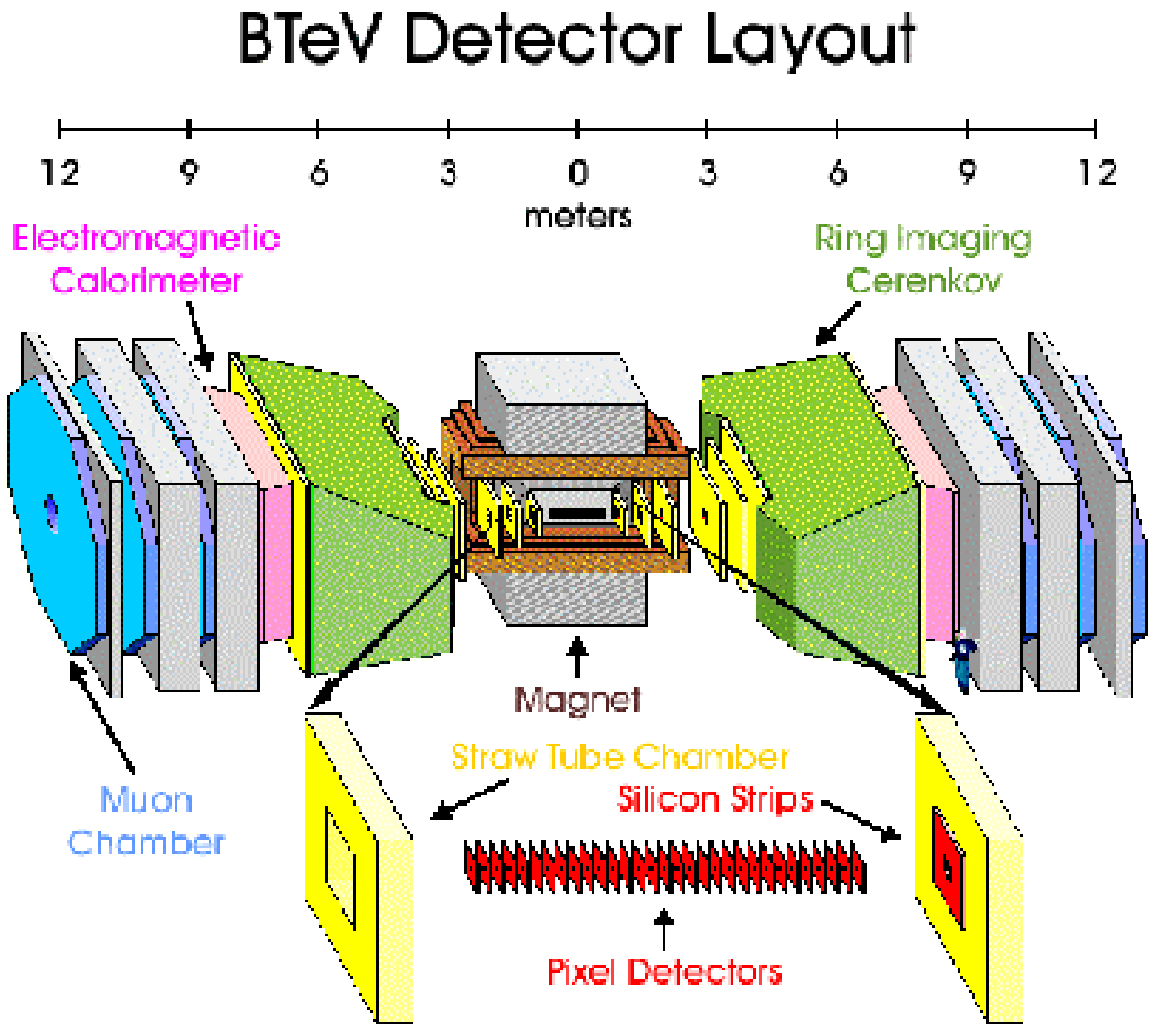
56 m^2 Silicon
Wafer size: 10 by 10 cm
# of Wafers: 6000 (incl. spares)
# of Channels: 4,404,480 channels
(260 μm pitch)

Forward tracker: Silicon Strip
Five disks uniformly spaced in z
Radiation length / layer = 1.0 %
Double-sided with 90 degree stereo, sigma = 7μm

Inner radii	Outer radii	Z position
4.0 cm	20.50 cm	27.1 cm
7.9 cm	46.75 cm	62.1 cm
11.7 cm	73.00 cm	97.1 cm
15.6 cm	99.25 cm	132.1 cm
19.5 cm	125.50 cm	167.1 cm

Vertex detector:CCD
5 layers uniformly spaced (r = 1.2 cm to 6.0 cm)
Half-length of layer 1 = 2.5 cm
Half-length of layers 2-5 = 12.5 cm
sigma_rphi = sigma_rz = 5 microns
Radiation length / layer = 0.1 %

The BTeV Detector



Comparison: Experience

- strip detectors are workhorses. Most large experiments use strip and most of the detectors come from Hamamatsu
- CCD and SDD have both one large device successfully completed.
- Hybrid pixels are in large demand for the future
- MAPS are presently the most promising future development

Comparison: Resolution

- generally the resolution achieved with existing devices is very similar (between 20-50 micron in the sensitive direction)
- the resolution goals for future devices reach down to less than 10 micron for all technologies)

Comparison: Scalability

- strip detectors are proven to be scalable to hundreds of m^2
- drift detector layout easiest to scale
- presently MAPS are R+D effort
- CCD cryo systems and electronics and hybrid pixels electronics not easily scalable

Comparison: Readout speed

- CCD and MAPS have same principle of moving information around. Could be faster if column-wise readout (increase in cost and extra layout R+D
- SDD are slow because of drift time. Can be increased by increasing HV, but never as fast as hybrid pixel or strip
- hybrid pixel and strip can provide level 0 trigger information (readout in 100 ns).

Comparison: Radiation length

- what has been achieved with various technologies (CCD, strip, drift) is all very comparable (about 1-2% per layer incl. support and cooling)
- stretched CCD or MAPS could be as low as 0.1% per layer
- SDD and strip detectors can be thinned to as low as 0.2% per layer (w. support and cooling probabyl 0.5%).
- hybrid pixels will always have the disadvantage of a separate sensor and electronics layer. Only the electronics layer can be thinned after processing

Comparison: Radiation hardness

- CCD radiation softness still a major R+D issue
- SDD are made of high resistivity NTD material, good to about 500 kRad
- hybrid pixel, strip, and MAPS can use deep sub-micron (DSM) electronics good to 10 MRad (but BELLE and CLEO both suffered from radiation damage at much lower rad. levels)

Comparison: Cost

- generally the main cost is in the electronics. Granularity determines cost. (SDD is 1-d readout for 2-d information with large pitch, MAPS is one channel per pixel)
- sensor cost is small item, but SDD is most expensive

Experiences with existing detectors

- CCD: small size detector, superior resolution, radiation soft, slow, difficult integration
- SDD: medium size detector, excellent resolution, slow, easy integration, difficult control of environment
- Strip: medium to large scale detector, good resolution, fast, easy integration and operation, reliable
- ALL: STARTUP PROBLEMS

Startup problems of latest generation Silicon detectors

- CDF: 5% dead, 35% need repair (cooling)
- D0: 2% dead, 15% need repair (cabling and connectors)
- STAR: 3% dead, 20% need repair (shielding, high noise)
- BELLE: 100% dead (radiation damage)
- CLEO: 10% dead, 50% need repair (aging due to radiation damage)
- BABAR: 5% dead

Experiences

- CDF, D0: do not mix and match technologies, use single-sided rather than double-sided silicon strip
- CLEO (strip), ALICE (drift): test sensors for radiation damage before use in detectors

Existing Capabilities

- we can produce detector systems that contain up to 200 m^2 of Silicon
- we can reduce radiation lengths to below 1% per layer
- we can build Silicon detectors that contribute to level 0 trigger.
- we can build detector systems that are exchangeable within a year's time and still cost and performance competitive (BELLE)

Concerns

- are there enough Silicon foundries that are interested to produce special batches ? Hamamatsu seems to provide almost all strip detectors without delivery problems but what about other technologies ?
- can a difficult technology (i.e. SDD) be mass-produced on a reasonable time scale ?
- can an easy technology (i.e. strip) be assembled into a large device on a reasonable time scale ?

Something to keep in mind

- this is a detector R+D workshop but the next generation detectors requires hopefully very little R+D and is based on proven technology (e.g. strip or pad) or is using detectors in production (e.g. hybrid pixels or drift)

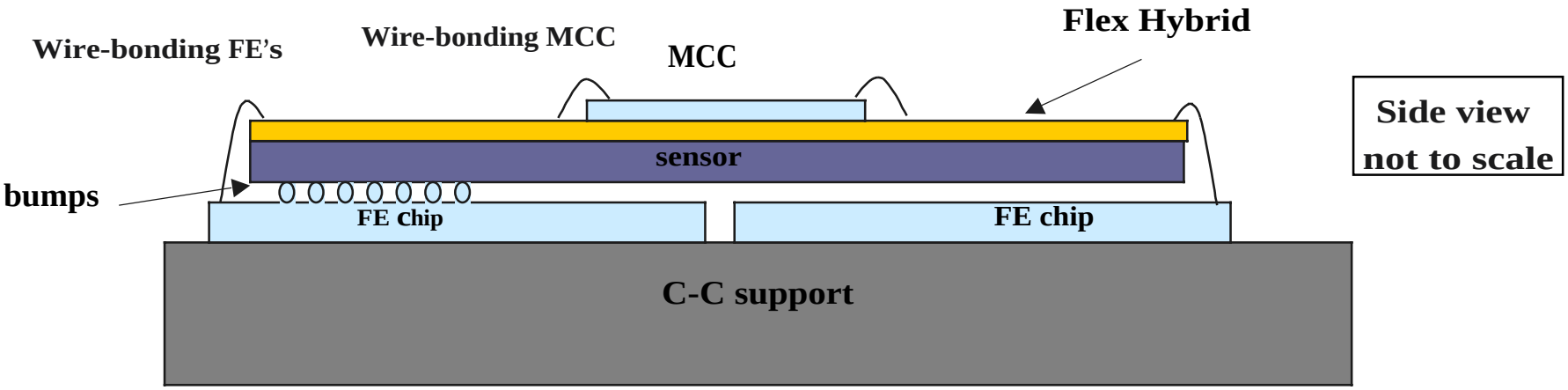
- new concepts (e.g. very large devices based on drift detectors or small devices based on MAPS or new CCD's will need R+D but will also require long timelines for R+D plus construction phase)

Summary

- We have a handful of potential upgrade projects for RHIC that are based on Silicon detectors
- We can choose from 5+ different technologies. Each of them has proponents and an active community. Each has different strengths and weaknesses.
- This workshop will help us in making our choices in terms of technology and upgrade priorities

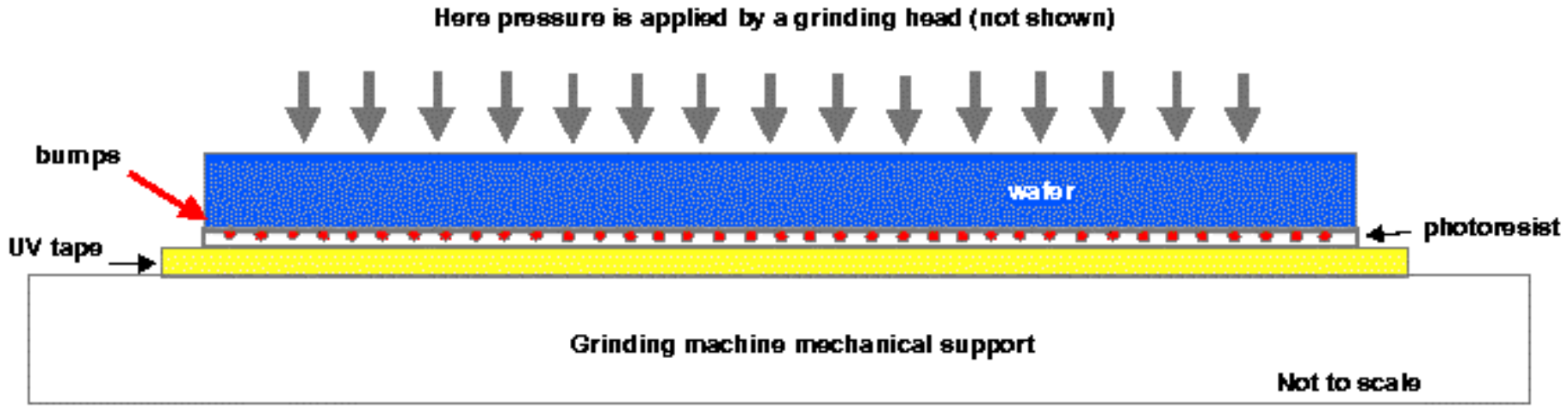
ATLAS Pixel Modules

- Modules are the basic building elements of the detector (1456 in the barrel + 288 in the end-caps).
- Each module has an active area of 16.4 mm x 60.8 mm.
- The sensitive area is read out by 16 FE chips, each serving a 18 columns x 160 row pixel matrix.
- The 16 FE chips are controlled by a Module Controller Chip (MCC).
- A Flex-Hybrid circuit glued on the sensor backside provides the signal routing between the 16 FE chips and the MCC. It also provides power routing for the FE's, MCC and sensor.



Thinning the electronics

- Bumping can be on one side only or on two sides. UBM must be on both sides.
- After bumping, thinning of electronics wafers might be envisaged (to reduce dead material). This is a large scale standard industrial process (mechanical backgrinding); also plasma thinning can be done, but it is more exotic (slower, more expensive).
- Thinning of (In and PbSn) bumped 6" wafers to 150 μm has been proven, it requires thin and uniform photoresist protection of bumps.

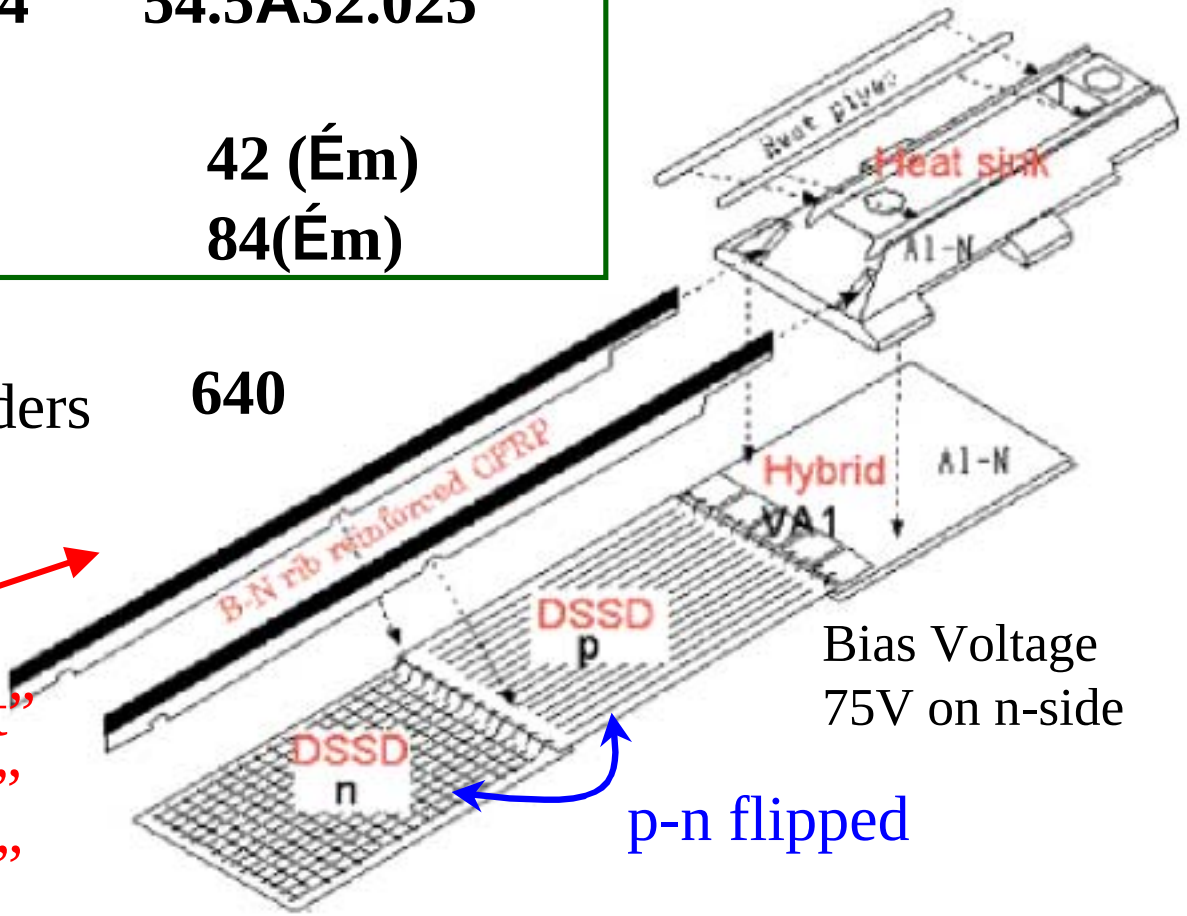


DSSD Ladders

DSSD (S6936 manufactured by HPK)		
	p-side (rϕ)	n-side (z)
Active area (mm^2)	53.5Å32.04	54.5Å32.025
Strip pitch	25	42 (Ém)
Readout pitch (ganged)	50	84(Ém)
# of readout	640	640

- Only 2 kinds of half-ladders ("short" and "long")

"Long" half-ladder
layer 1 : "short" + "short"
layer 2 : "short" + "long"
layer 3 : "long" + "long"



Bias Voltage
75V on n-side

Radiation Sickness

- Initially, efficiency in layer-1, r-ϕ, was ~60%.

  Lower than expected

  But other layers (r-ϕ, z) were ok
- First hint at true nature of problem from high-statistics mapping of silicon hits.
- r-ϕ efficiency shows structure on the wafer.
- Varying the detector/FE electronics settings within the possible range could not restore efficiency.

Time Evolution

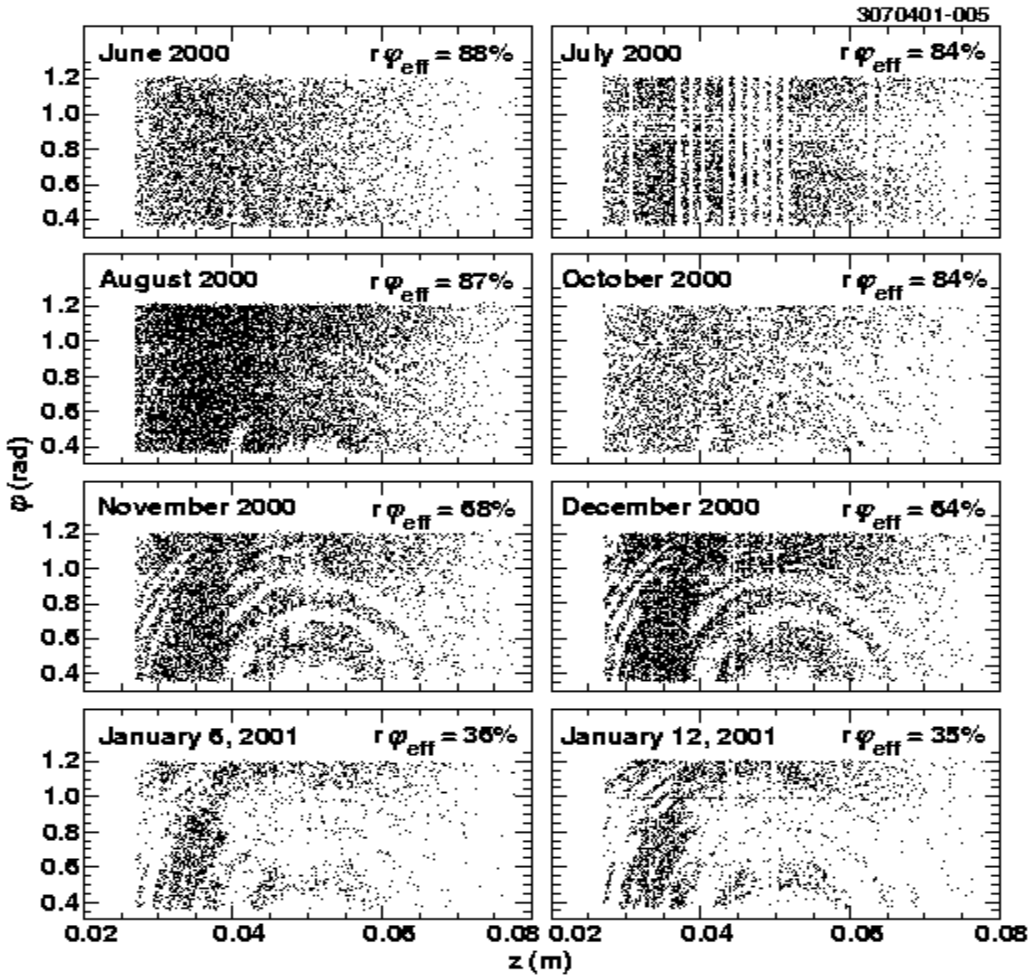
Example: a Layer-2 Sensor

- Problem(s) getting worse with time
- Affected now:

  Layers 1+2 r-ϕ

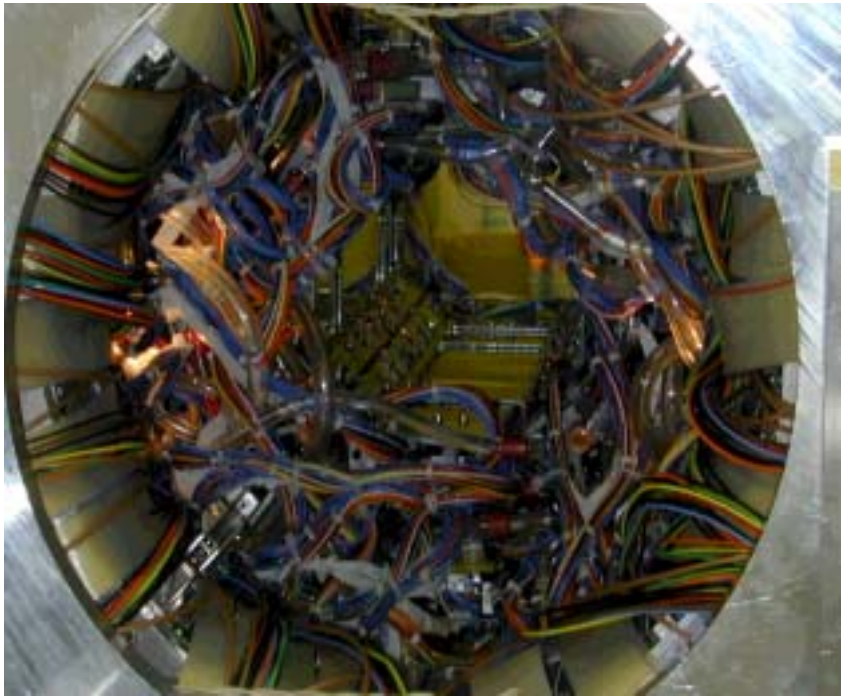
  Outer layers still ok,

  z-side still efficient
- Most likely explanation: Radiation damage to silicon sensors. Exact mechanism unknown.



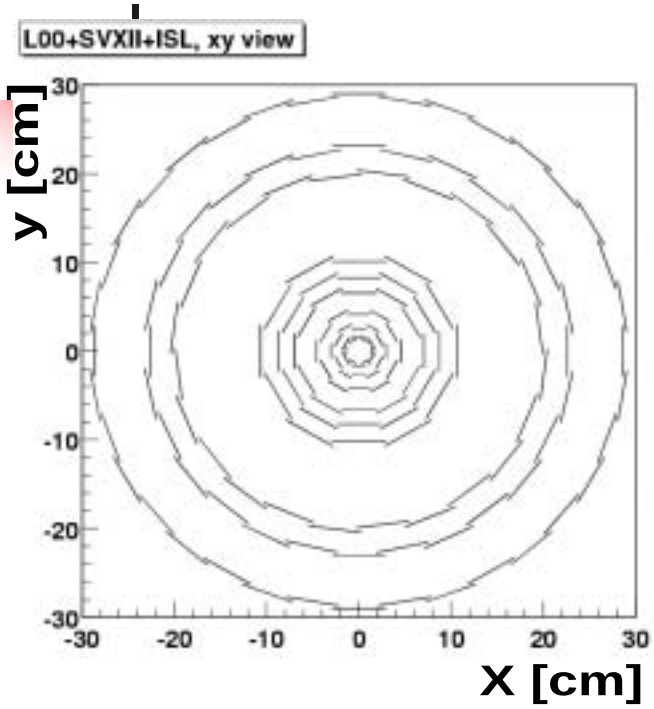
The SVT in STAR

Construction
in progress



Connecting
components

Detector Layout



Basic concept:

- **1 layer (L00) very close to the beam: improve IP res. & b-tag**
- **5 layers (SVXII) very compact in r,ϕ,z: 3D vertexing & tracking**
- **1 central/2 forward layers (ISL) at large radius: tracking**

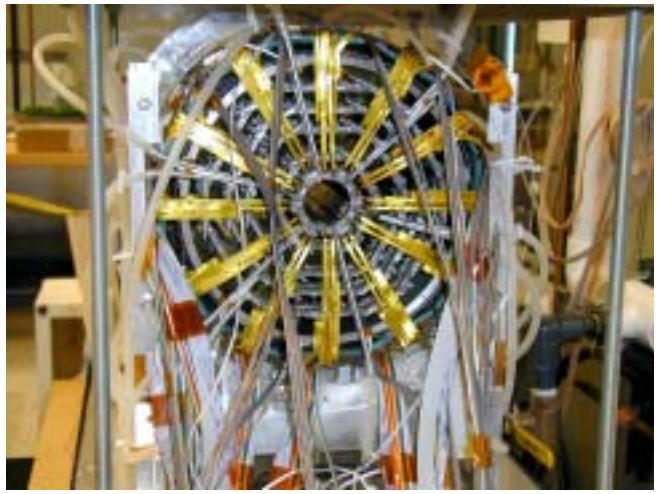
ÿ Use L00/SVXII for vertexing & L2 trigger: high density & precise alignment crucial!

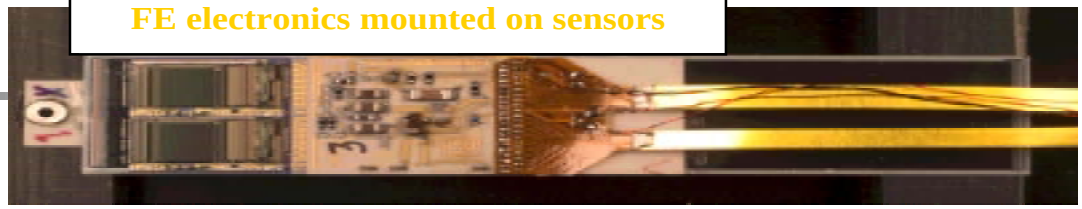
ÿ Use ISL for tracking: simpler design; precise alignment not that important

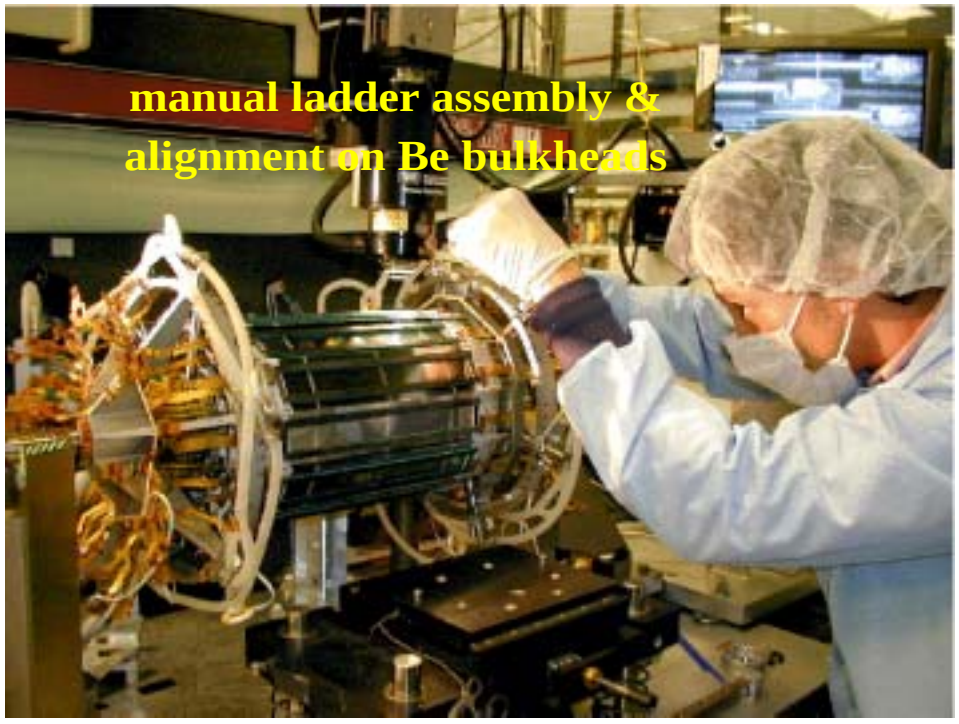
376 modules, 722432 RO channels ⇒ **silicon detector is ~15 times larger than in Run1!**

Detector Assembly – SVXII (1)

- **Very compact design: 5 DS layers within 10.5cm**
- **3 barrels: support & cooling via Be bulkheads**
- **Portcards mounted outside of barrels**







Detector Assembly – SVXII (2)

Lessons learned:

- very complicated design, each layer is unique:
  - ÿ 5 DS silicon designs
  - ÿ 6 hybrid designs / 10 hybrid types
- difficult assembly:
  - ÿ quarter ladder: sensor/hybrid sandwich with ϕ/z jumper
  - ÿ full module: 2 quarter ladders + 2 sensors
  - ÿ difficult to handle + a lot of repair work necessary (25% of all modules)
  - ÿ average number of dead channels: 3%/2% on ϕ/z side
  - ÿ required 20 work hours per module (~4 technicians for 9 months)

work in “pipeline mode”; minimize number of “flavors”; consider SS silicon

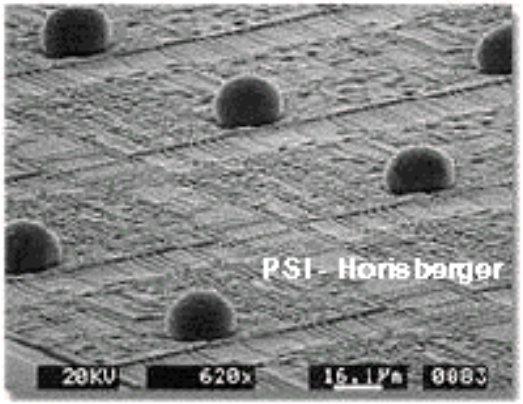
Insertable Layout for ATLAS pixel

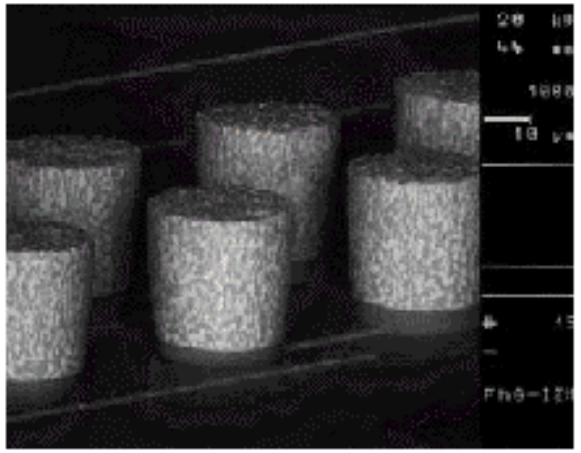
- Pixel detector layout and design have been modified over the last year to cope with delays in radiation-hard integrated circuit electronics.
- Pros:
  - Complete Pixel detector can be inserted or removed with remainder of Inner Detector in place i.e. as late as possible for initial installation.
  - The “insertable” concept will also facilitate maintenance, repair and upgrades.
  - Reduced number of modules (-17%)=> less time to produce them.
  - Transverse impact parameter resolution is similar to that expected by the previous layout.
- Cons:
  - Smaller external radius (14.2cm⇶12.2cm).
  - Worse material distribution (especially for high η).
  - ~2% of tracks with less than 3 points.

- Results as follows:

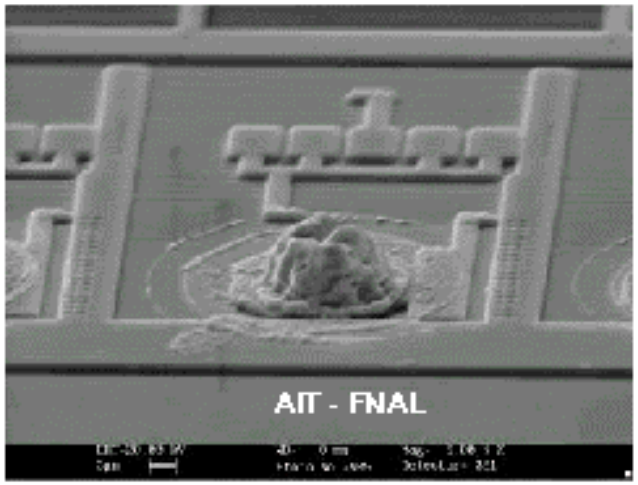
Indium

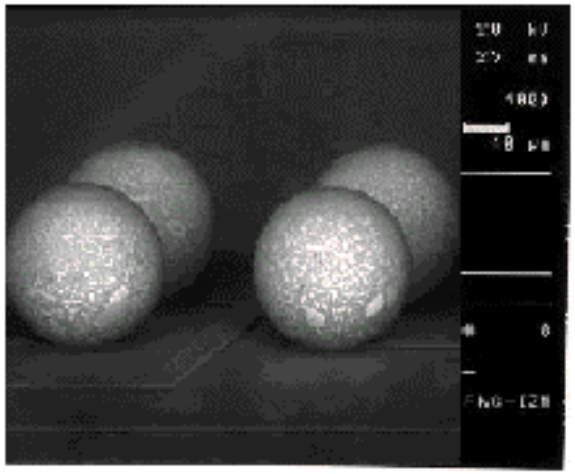
PbSn





After electroplating



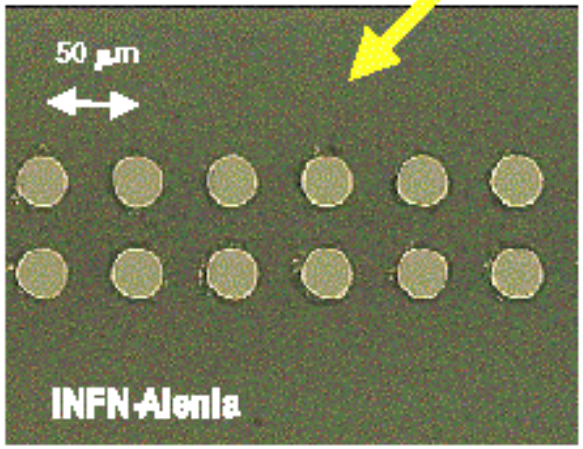


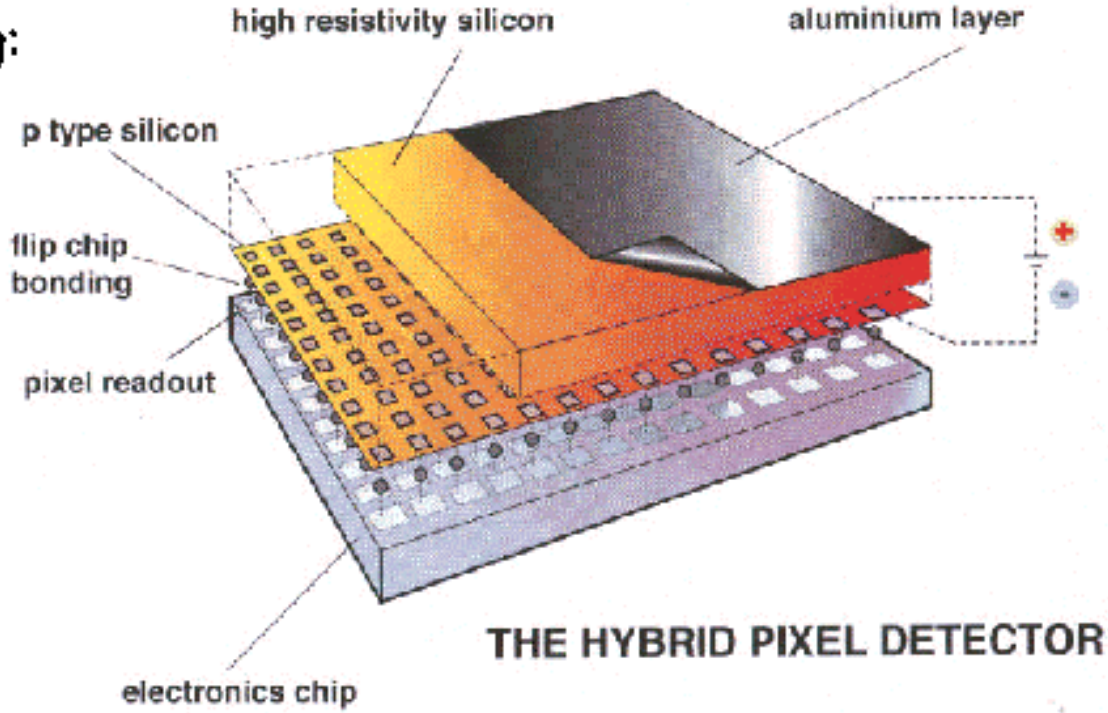
courtesy
IZM, Berlin

After reflow

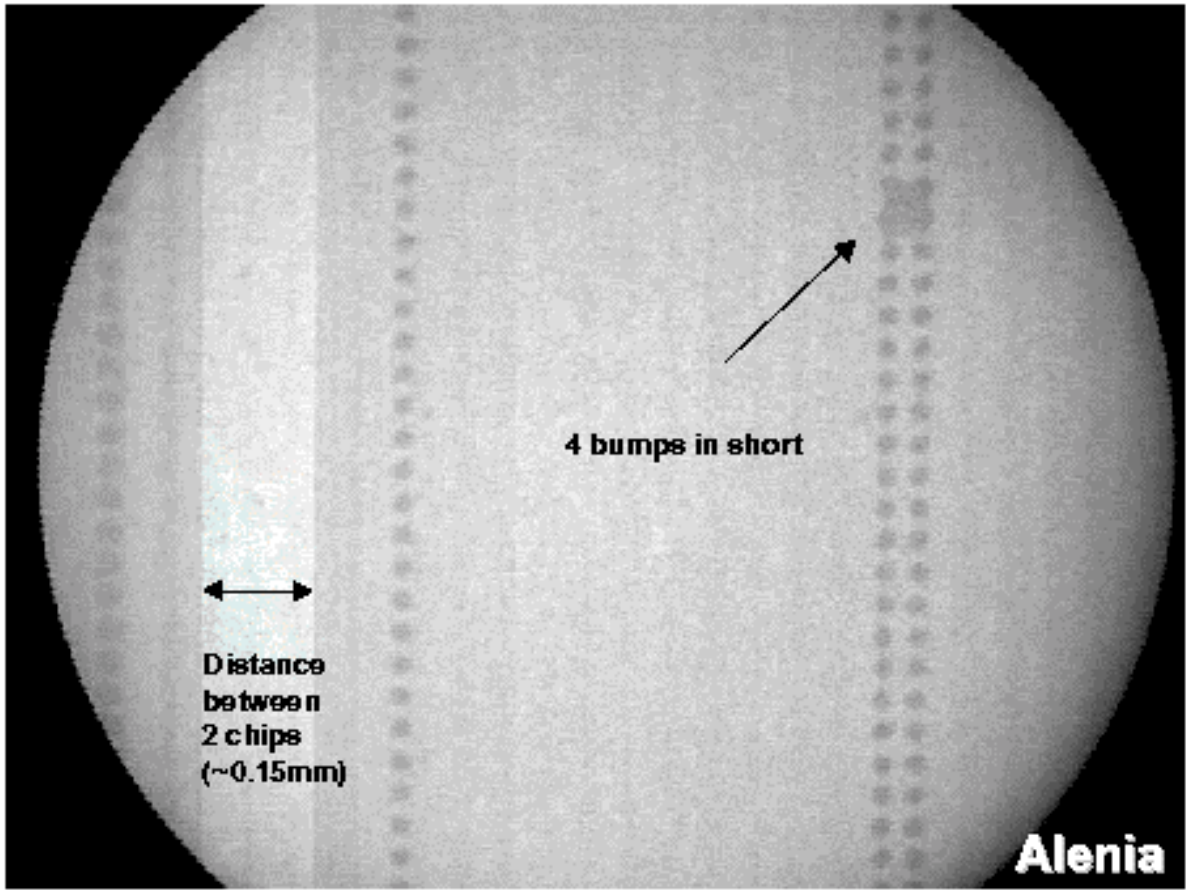
- Finally wafers are diced and eventually the dies are tested again to have KGD to start with (if 99% yield per die, 0.99^{16}= 0.85 yield per 16 chip module).
- The final step is the flip-chip where:
  - the mating chips are faced with ~μm accuracy
  - P and/or T are applied to fuse metal and establish connections

- Once chips&sensor are mated we get the following:
  - if we look trough and substrates are made of glass





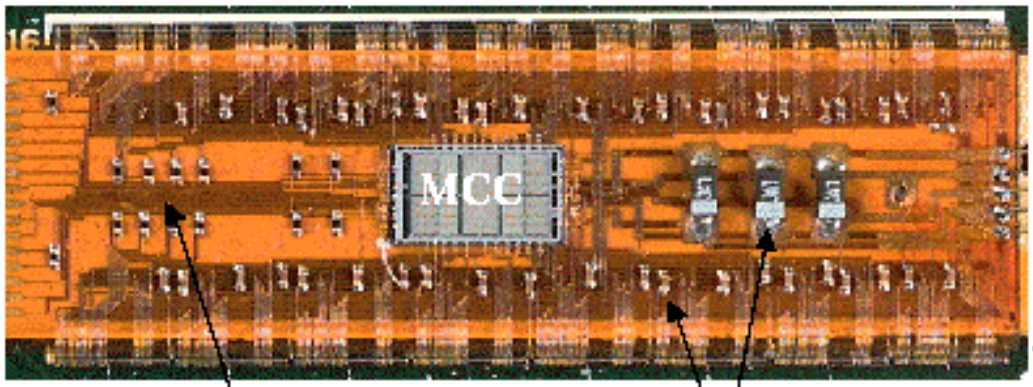
- Moreover the validation of the bump/flip process is only possible either through a microfocussed x-ray machine or by a full test of the module under needles in a probe station.

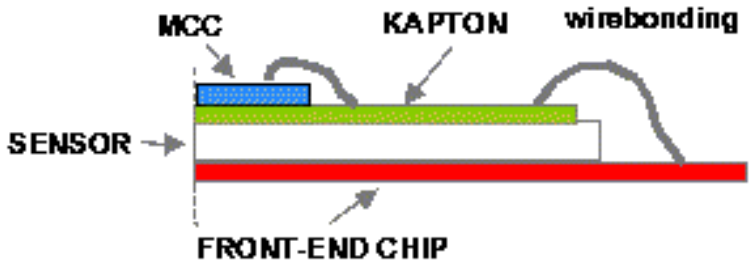


- Fine focussed x-ray spot defects
  - aside an example of an Alenia module. The region between two chips is shown.

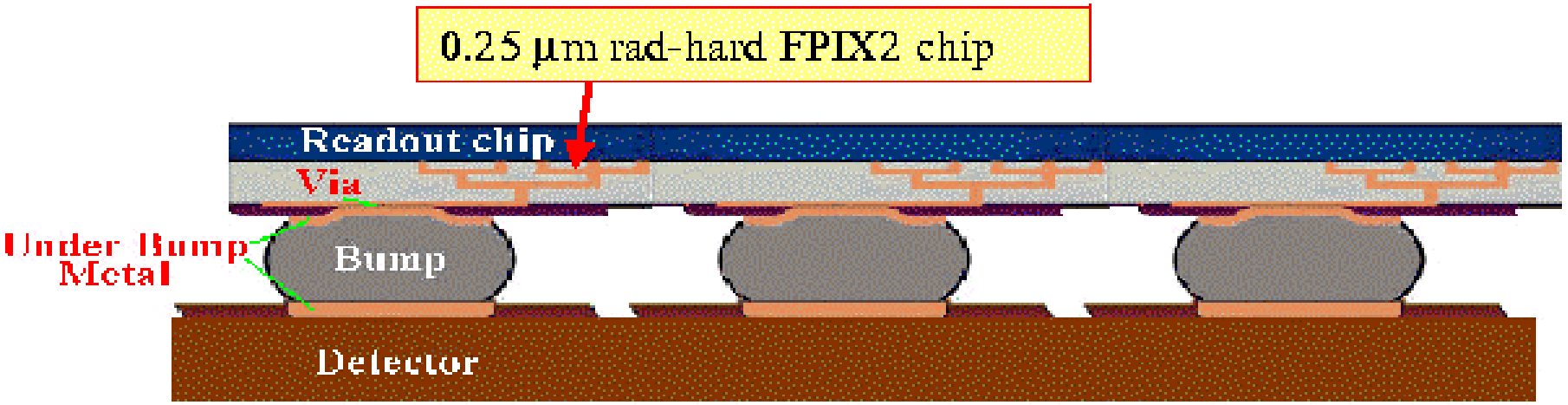
- Configuration and control signals must be provided together with power supplies (low and high voltages) and their decoupling. The data output stream must be organised and transmitted out.
  - The most common solution is to include this higher level connectivity on a thin kapton substrate to be glued on the backside of the sensor tile.
  - Load resistors, decoupling capacitors and T-sensors are mandatory on kapton together with low/high voltage & signals routing
  - Data organization and data transmission can be on (all or in part). Most designs foresee a Module Control Chip (MCC) where both functions are done.

Sketch of side view edge





Hybrid Silicon pixel devices



- Independent development and optimizations of readout chip and sensor
- n^+ pixels on n-type substrates: inter-pixel insulation technology under investigation
- Bump-bonding of flipped chip: 2 technologies being considered: Indium (In) and solder (SnPb)